ELLIOTT
905

905 DIGITAL COMPUTER SYSTEM
FUNCTIONAL SPECIFICATION

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Chapter 1:   905 SYSTEM FUNCTIONAL SPECIFICATION

1.1   INTRODUCTION

The 905 Computer has an 18-bit word length and has been designed as a more powerful version of the original Elliott 903, using contemporary technology.

It is "upwards program compatible" with the 903, i.e. programs written for the 903 can be run on the 905 without alteration, and also "upwards interface compatible" in that peripheral devices designed for the 903 may be attached to the 905.

The 905 architecture is identical with the 920C military computer, providing facilities for direct store access and multiple processor complexes.
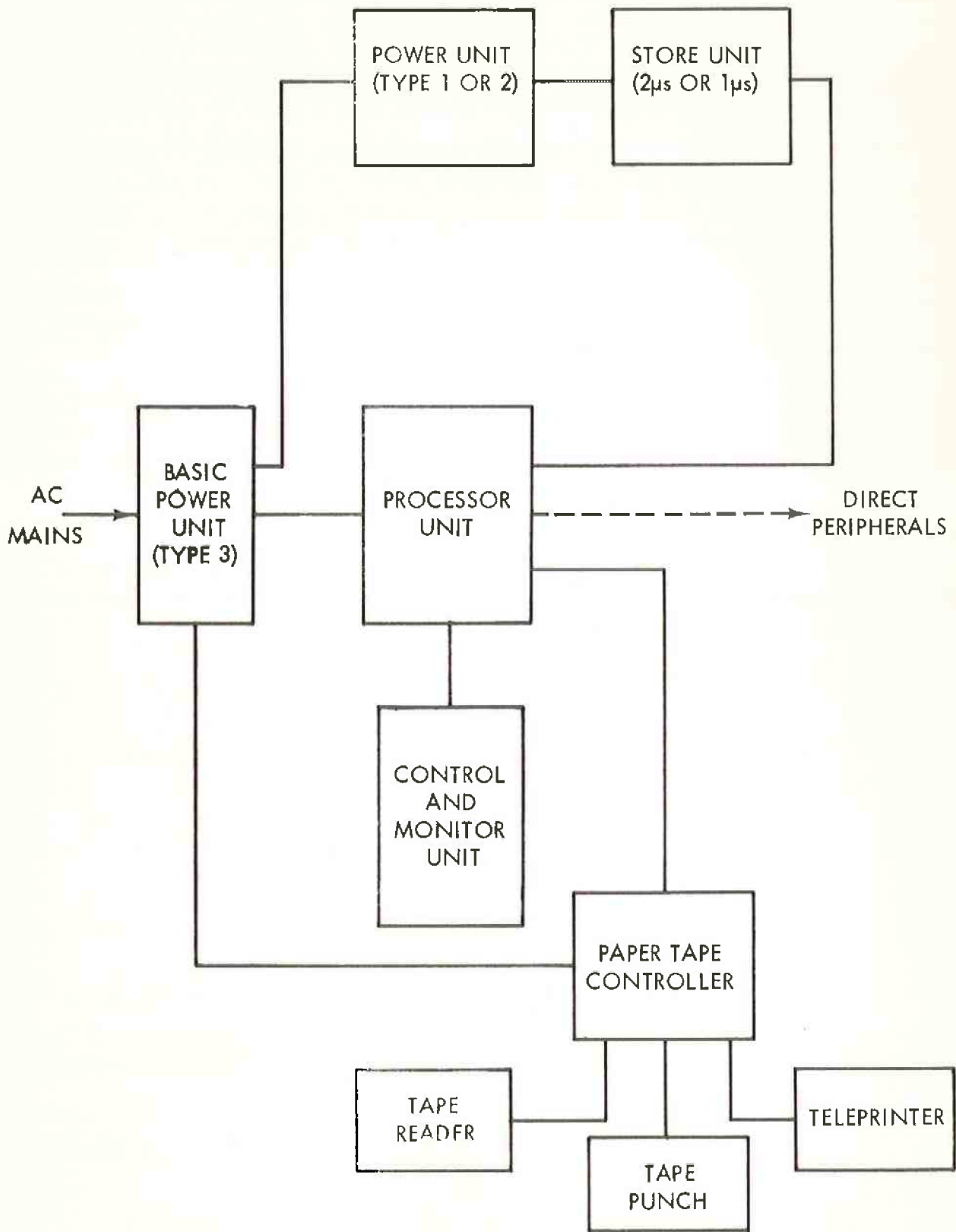
Fig. 1

BLOCK DIAGRAM-STANDARD 905 SYSTEM

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Chapter 2:   STANDARD 905 SYSTEM

2.1   CONFIGURATION (see Fig. 1)

A standard 905 system consists of the following:-

(a)   Processor unit

(b)   Store 8192 words, $1\mu s$ or $2\mu s$

(c)   Power unit

(d)   Control and monitor panel

(e)   Paper tape control unit

(f)   Teleprinter   } Options

(g)   Tape reader

(h)   Tape punch

2.2   WORD LENGTH AND FORMAT

Numbers and instructions in the 905 system are each 18 bits in length.

Numbers are represented in fractional form, negative numbers being held in "two's complement" form. They will thus be in the range -1 to $1-2^{-17}$. The significances of individual bits in a number are shown below:-

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
-1	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}

Instructions are of the single address type, one instruction being represented by a 18-bit word. An instruction word consists of three parts:

Modifier (B) - 1 bit - specifies whether modification is required

Function (F) - 4 bits - specifies the operation to be carried out

Address (N) - 13 bits - specifies, generally, the store address of one operand.

The instruction format is as shown below:-

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
B	F				N												

2.3   STORE

The store of a standard 905 system holds 8192 words each of 18 bits; these are referred to by addresses in the ranges 0 to 8191.

Two types of store are available, having nominal cycle times of 1μs and 2μs.

In the case of the 1μs store, operation is checked by means of a parity bit which is stored with each word; on writing into the store this bit is set to give the whole word odd parity. If even parity is detected on reading from the store the computer may stop (see section 2.7.4).

The 1μs store also incorporates a block protection facility. The store is divided into blocks of 1024 words each; when the protection (or "lock-out") facility is brought into operation, selected blocks of store are made "read-only" and their contents cannot be changed. If the program attempts to write into a location in a protected block the computer may stop (see section 2.7.4). The selection of protected blocks is done by external connections.

2.4   REGISTERS

The following registers are used by instructions:

A Register: This is an accumulator with a capacity of 18 bits which is used to hold the result of most operations.

Q Register: This is a register with a capacity of 18 bits which is used to hold information temporarily during a computation, and also as an extension of the accumulator for numbers containing more than 18 significant bits. In this case it extends the less significant end of the accumulator by 17 bits, using bits 2 to 18 of the Q register. The register used in this way is known as the Auxiliary register.

B Register: This 18 bit register holds the number which is added to the N bits of the instruction to form the address if the B bit of the instruction is a 'one'.

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S Register: This register, with a capacity of 17 bits, controls the extraction of instructions from the store; it is incremented as each instruction is extracted from the store so that instructions are obeyed in numerical sequence. In the standard system, having 8192 words of store, only 13 bits of S are used.

H Register: This register, of one bit only, controls the manner in which instructions address locations of the store. It is only relevant when the store is extended beyond 8192 words.

2.5 PROGRAM LEVELS AND INTERRUPT FACILITY

Provision is made for four program priority levels, which are arranged to operate on an interrupt basis. If, while the computer is running, an interrupt signal is received for a higher priority program, the program currently being obeyed will be temporarily suspended as soon as the instruction (other than function 0) currently being obeyed is completed and the higher level program will be obeyed. When this higher level program is terminated by a program terminate instruction the computer will revert to the lower level program and continue from the point at which it was interrupted.

A sequence control register (S register), an address mode indicator (H) and modification register (B register) are provided for each program level. These registers are held in the computer store in location 0 to 7 as follows:

	S Register		H Register		B Register
Program level 1	0 (digits 1-17)		0 (digit 18)		1
2	2	"	2	"	3
3	4	"	4	"	5
4	6	"	6	"	7

Program level 1 is the highest priority and cannot be interrupted.
Program level 2 may be interrupted only be level 1.
Program level 3 may be interrupted by levels 1 and 2.
Program level 4 may be interrupted by levels 1, 2 and 3.

Interruption occurs as a result of a signal received from a peripheral equipment.

The S and H registers corresponding to the program level currently in use are held in the processor for fast access, being automatically stored and replaced by previously stored values when interruption or termination occurs.

The A and Q registers must be stored by program instructions at the beginning of the higher priority program, and restored before termination. At the initial start-up of the program system the starting address for the appropriate programs must be placed in locations 2, 4 and 6. This is normally done by a program operating on level 1 entered by the "Jump" control (see section 2.7.3).

2.6 INSTRUCTION REPERTOIRE AND OPERATION TIMES

2.6.1 In the tables that follow, the effects of instructions are defined in terms of the initial and final contents of registers and store locations as follows:-

S, A, Q, B refer to the contents of the various registers.

AQ   refers to the contents of A and Q regarded as a double-length number.

B, F, N   refer to the parts of the instruction word being obeyed.

Numbers in square brackets indicate particular bits of registers, e.g. A [1-8] means bits 1-8 of register A.

Primes indicate the contents of store locations specified, e.g., N' means the contents of store location N.

M means the address of the modifier register of the current program level, i.e., location 1, 3, 5 or 7 depending on which priority level is currently operating.

:= means "is made equal to".

The instruction times quoted are nominal figures subject to a tolerance of ± 15%.

2.6.2   Un-modified Instructions (B = 0)

(a)   Inter-register transfers

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N
A to B	B:= A		{4.1	6.1	15	7174
			{3.3	5.3	5	M
A to Aux.	Q [2-18] := A [1-17]		3.7	4.7	15	7172
B to Q	Q:= B		3.6	6.6	0	M
S to B	B [1-13] := S [1-13] B [14-18] := 0	Q [14-17] := [14-17] Q [1-13] := 0	3.3	5.3	11	M
B to A	A := B		(4.1	6.1	15	7175
			(2.4	4.4	4	M
Aux. to A	A [1-17] := Q [2-18] A [18] := 0		3.7	4.7	15	7173
Aux. to B	B [1-17] := Q [2-18] B [18] := 0		3.3	5.3	3	M

(b) Transfers between registers and store

Name	Operation	Other effects	Time		Instruction	
			1µs store	2µs store	F	N
Read	A:= N'		2.4	4.4	4	N
Load B	B:= N'	Q:= N' (no interrupt following this instruction)	3.6	6.6	0	N
Load Q	Q:= N'	B:= N' (no interrupt following this instruction) OR A:= N'-A	3.6	6.6	0	N
Write	N':= A		3.3	5.3	2	N
Store S	N' [1-13] := S [1-13] N' [14-17] := 0	Q [14-17] := S [14-17]	3.3	5.3	5 11	N N
Store Aux.	N' [1-17] := Q [2-18] N' [18] := 0		3.3	5.3	3	N

(c) Arithmetic between Accumulator and B register

Name	Operation	Other effects	Time		Instruction	
			1µs store	2µs store	F	N
Add A to B	A:= A+B		2.4	4.4	1	M
Subtract A from B	A:= B-A	Q:= B	3.3	5.3	2	M
Multiply A by B	AQ:= AxB	Q [1] altered	10.2	12.2	12	M
Divide by B	A:= AQ ÷ B	Q:= AQ ÷ B	19.3	21.3	13	M
Collate A with B	A:= A and B		2.4	4.4	6	M

(d) Arithmetic between Accumulator and Store

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N
Add	A:= A + N'		2.4	4.4	1	N
Negate and add	A:= N' - A	Q:= N'	3.3	5.3	2	N
Multiply	AQ:= A x N'	A [1] altered	10.2	12.2	12	N
Divide	A:= AQ ÷ N'	Q:= AQ ÷ N'	19.3	21.3	13	N
Collate	A:= A and N'		2.4	4.4	6	N

(e) Transfer control

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N
Jump zero	if A = 0 then S := N		1.2	2.2	7	N
Jump	S := N		1.2	2.2	8	N
Jump negative	if A<0 then S := N		1.2	2.2	9	N
Count and test	B:= B+1 if B [1-13] = 0 then S:= S+2		5.3(B≠0) 6.2(B=0)	8.3(B≠0) 9.2(B=0)	15	7170
Test standard	if A>+$\frac{1}{2}$ or A<-$\frac{1}{2}$ or A = 0 then S:= S+1		2.9 (not standard) 3.8 (standard)	4.9 (not standard) 5.8 (standard)	15	7169

(f) Miscellaneous

Name	Operation	Other effects	Time		Instruction		Notes
			1μs store	2μs store	F	N	
Count in B	$B: = B+1$		3.6	5.6	10	M	
Count in store	$N': = N' + 2^{-17}$		3.6	5.6	10	N	
Shift left	$AQ: = AQ \times 2^N$		$2.9+0.9n$	$3.9+0.9n$	14	0 to 36	
Shift right	$AQ: = AQ \times 2^{N-8192}$		$2.9+0.9n$	$3.9+0.9n$	14	8156 to 8191	i.e. shift right 8192-N (=n) places
Terminate	Current program level terminated		7.4	11.4	15	7168	
Set relative	$H: = 0$		3.7	5.7	15	7176	used only in conjunction with extended store
Set absolute	$H: = 1$		3.7	5.7	15	7177	

(g) Input and output

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
Key input	A: = word generator		3.7	5.7	15	7171	
Tape input	A [9-18] := A [2-11] or A [8] := A [1] or character [8] A [1-7] := character [1-7]		5.5 (min)	6.5	15	2048	Acc shifted left 7 places and 8 bit character logically mixed in
Teleprinter Input	A [9-18] := A [2-11] or A [8] := A [1] or character [8] A [1-7] := character [1-7]		5.5 (min)	6.5	15	2052	-do- Input from tape reader when teleprinter not fitted.
Word input	A := input word		5.5 (min)	6.5m	15	0 to 2047	Input device and action selected externally by N[1-11]
Block input	A' = 1st input word (A+1)' := 2nd input word etc. (A+Q [1-12] -1)' := last word input.	A, Q altered	3.8+5.5n (min)	4.8+6.5n m	14	2048 to 4095	Input device and action selected externally by N[1-11]. No. of words input = Q [1-12] (=n).
Tape output	Character:= A [1-8]		5.5 (min)	6.5m	15	6144	
Teleprinter Output	Character:= A [1-8]		5.5 (min)	6.5m	15	6148	
Word output	Output word := A		5.5 (min)	6.5m	15	4096 to 6143	Output device and action externally by N [1-11]
Block output	1st output word := A' 2nd output word := A+1' etc. Last output word := (A+Q [1-12] -1)'	A, Q altered	3.8+5.5n (min)	4.8+6.5n m	14	4096 to 6143	-do- No. of words output = Q [1-12]

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2.6.3   Modified Instructions

When the B digit of an instruction is 1, the instruction is said to be "modified"; the effect of this is that the address of the instruction is altered by the addition to it of the contents of the B register. In the standard system, with 8192 words of store, the resulting address must not be outside the range 0 to 8191.

In the following tables all useful modified instructions are listed.

X is used to mean B + N.

(a)   Transfers between registers and store

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N
Read	A:= X'	Q altered	3.6	6.6	4	N
Load B	B:= X'	Q:= X'	4.8	8.8	0	N
Load Q	Q:= X'	{ B:= X'	4.8	8.8	0	N
		A:= X' - A			2	N
Write	X':= A	Q altered	4.5	7.5	5	N
Store S	X':= S [1-13]	Q:= S [14-17]	4.5	7.5	11	N

(b) Arithmetic between registers and store

Name	Operation	Other effects	Time		Instruction	
			1μs store	2μs store	F	N
Add	A:= A + X'	Q altered	3.6	6.6	1	N
Negate and Add	A:= X' - A	Q:= X'	4.5	7.5	2	N
Multiply	AQ:= A x X'		11.4	14.4	12	N
Collate	A:= A and X'	Q altered	3.6	6.6	6	N

(c) Transfer control

Name	Operation	Other effects	Time		Instruction	
			1μs store	2μs store	F	N
Jump zero	if A = 0 then S:= X	Q altered	1.2(A≠0) / 2.4(A=0)	2.2(A≠0) / 4.4(A=0)	7	N
Jump	S:= X	Q altered	2.4	4.4	8	N
Jump negative	if A<0 then S:= X	Q altered	1.2(A>0) / 2.4(A<0)	2.2(A>0) / 4.4(A<0)	9	N

(d) Miscellaneous

Name	Operation	Other effects	Time		Instruction		Notes
			1μs store	2μs store	F	N	
Count in store	X':= X' + 2^{-17}	Q altered	4.5	8.5	10	N	
Word input	A:= input word	Q altered	6.7 (min)	7.7 (min)	15	N	X in range 0-2047, device and action selected by X [1-11].
Word output	Output word:= A	Q altered	6.7 (min)	7.7 (min)	15	N	X in range 4096-6143, device and action selected by X [1-11]

2.6.4   Program Compatibility

Programs written for the 903 computer
using the instruction code as defined in the 903 Manual (Volume 1, Part
2, Section 2, Chapter 3) can be accepted unchanged by the 905. This
applies to the Symbolic Input Routine (SIR), the ALGOL and FORTRAN
compilers and all other standard 903 software.

2.7   CONTROL AND MONITOR UNIT (see Fig. 2)

2.7.1   Master Switch

This switch, operated by a Yale-type key,
has three positions - AUTO, MANUAL and TEST. When it is in the
AUTO position only the on/off switch is operative, when in the MANUAL
position sufficient controls for the routine operating of developed
programs are operative. When in the TEST position, all controls are
operative.

2.7.2   Power Controls and Indicators

The ON/OFF switch controls the power
switching for 905 and associated equipment.

When switched on the power supplies are
sequenced on in such a manner as to retain store contents; the computer
then either

        (a)   if the master switch is in MANUAL or
                     TEST enters the RESET (quiescent) state
                     (see section 2.7.3(b))

or   (b)   if the master switch is in AUTO starts
                     obeying program, on level 1, at
                     location 8177.

When switched off the power supplies are
sequenced off in such a manner as to retain store contents.

The POWER ON lamp is illuminated
(colour green) whenever the ON/OFF switch is in the ON position and
the mains supply is connected.

The READY lamp is illuminated (colour
green) when the power supplies have sequenced on correctly.

2.7.3 Manual Group Controls and Indicators

These controls are operative in the MANUAL and TEST positions of the master switch; the indicators are always operative.

(a) The NUMBER GENERATOR switches comprise 18 two-position switches which may be set to represent the binary digits of a computer word. This word may be used:-

(i) As a computer input, read by a 15 7171 instruction.

(ii) As a starting address (in the range 0 to 8191) in conjunction with the JUMP control (see below).

(iii) As a word to be placed in the A register (see section 2.7.4).

(iv) As an instruction to be obeyed (see section 2.7.4).

(b) The RESET push button is used to restore the computer and associated equipment to their initial state, referred to as the "reset" state. The RESET lamp, incorporated in the push button, is lit as long as the state persists. The RESET state is terminated as follows: when the master switch is set to AUTO the state is terminated automatically in the switch-on sequence; when the switch is set to MANUAL the state is terminated by use of the JUMP control. When the master switch is set to TEST, the state is terminated:

(i) by use of the JUMP control

(ii) by use of the RESTART control when either of the ENTER or OBEY switches are set to "single" or "run" (see section 2.7.4).
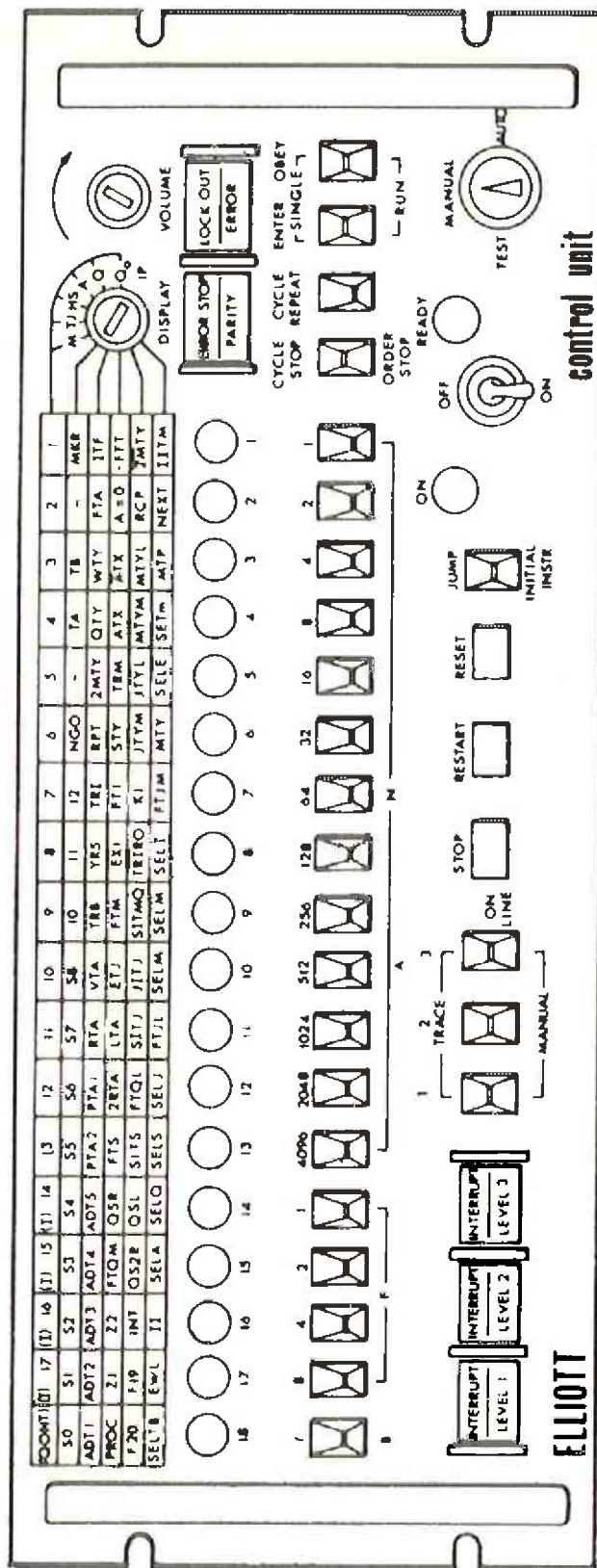
Fig. 2 905 COMPUTER CONTROL AND MONITOR PANEL

(c)   The JUMP control is a three-position switch biassed to its central position. When raised instantaneously from its central position it causes the computer to start obeying program, on level 1, at the address set on NUMBER GENERATOR keys Nos. 1-13.

When lowered it causes the computer to start obeying the INITIAL INSTRUCTIONS at location 8181.

The H register is cleared when this control is used.

(d)   The STOP push button allows the computer to be stopped at the completion of an instruction. The STOP lamp, incorporated in the push button, is lit when this happens and remains lit until the computer resumes operation.

(e)   The RESTART push button causes the computer to resume obeying the program at the point where it was stopped.

(f)   Interrupt controls

These controls comprise three illuminated push button microswitches and three associated level key switches. One push button switch and one key are associated with each of the three program levels, 1, 2 and 3.

When a key switch is down, the associated level will be set to Manual and external interrupt signals will not be recognised. When set to the up position, a permanent interrupt condition will be generated for use with the TRACE program.

In the intermediate position, the switches will allow on-line operation of the computer, i.e., it will recognise external interrupt signals.

The push buttons will only be effective when the corresponding level is set to

'manual'. In this case operation of the button will generate one interrupt condition.

The upper half (red) of a push button is lit when the computer receives an interrupt demand on that level. The lower half (green) will light when the corresponding program level is in operation.

NOTE: The master switch has the following effects when in the AUTO position:

Number generator - inoperative. An input instruction which reads the number generator will place a constant (non zero) in the accumulator.

Reset
Jump
Stop
Restart } - inoperative

Interrupt switches and push buttons - inoperative

External interrupt signals - enabled (i.e. as normal position of switch).

2.7.4   Test Group Controls and Indicators

These controls are only operative in the TEST position of the master switch; the indicators are always operative.

(a)   ENTER switch. This is a three-position switch, locking in each position; it permits a word set up on the NUMBER GENERATOR to be copied into the A register, the computer performing this operation instead of obeying an instruction. When the switch is in the "run" position the operation is performed continuously, once initiated by the RESTART button; when the switch is in the "single" position the operation is performed once each time the RESTART button is operated.

(b)   OBEY switch. This is a three-position switch locking in each position, it permits a word set up on the NUMBER GENERATOR to be obeyed as an instruction by the computer. When the switch is in the "run" position the instruction is obeyed continuously, once initiated by the RESTART button; when the switch is in the "single" position the operation is performed once each time the RESTART button is pressed.

(c)   STOP MODE switch. In the lowered position of this control the computer will be set to the 'Order Stop' state, in which it will obey a stored program one instruction at a time. Each successive order is initiated by operation of the 'RESTART' button.

In the raised position, the computer will be set in the 'Cycle Stop' state, in which the computer obeys successive steps in the microprogram each time 'RESTART' is operated. The 'STOP' lamp will be illuminated when the control switch is raised or lowered, remaining alight until normal operation is resumed, on selecting the centre switch position.

(d)   CYCLE REPEAT switch. When this key is set to the raised position, the computer will obey a single instruction in the microprogram repeatedly.

If 'Cycle Stop' is set, repetition will occur each time the RESTART control is operated. If 'Cycle Stop' is not set, repetition occurs continuously.

(e)   LOCKOUT switch and lamp. This is an alternate action push button switch. When the push button is depressed to light the 'Lockout' lamp (upper half, green) store protection is in operation. When the lamp is not illuminated, store protection is disabled.

The LOCKOUT ERROR lamp (lower half, red) is illuminated when the computer stops because of an attempt to overwrite a protected word.

(f)   ERROR STOP switch and lamp. This is an alternate action push button switch. When the push button is depressed and the lamp (upper half, yellow) is illuminated the processor will stop if a store parity error is detected or when store protection is in operation and an attempt is made to overwrite a protected word. When the lamp is not illuminated the processor will not stop on errors.

PARITY LAMP. This is illuminated (lower half, red) when the computer stops on a store parity error.

NOTE: The master switch has the following effects when in the AUTO or MANUAL positions:-

Enter Obey Stop Mode Cycle Repeat	- inoperative
Lockout	- inoperative (store protection operative)
Error Stop	- inoperative. The computer will continue to run in the event of a parity or lockout error.

2.7.5   Monitor Facilities

These are available in any position of the

master switch.

(a)   MONITOR DISPLAY switch and indicator lamp. The eighteen indicator lamps, in conjunction with the eleven position selector switch, enable the state of all central processor registers, important staticisers, and control logic waveforms to be displayed to the operator.

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The waveforms available are listed below:-

Display Switch
Position   Waveform Groups Displayed

1   Register Bits P1-P13; I14-17; Qo
2   Register Bits Q1-18
3   Register Bits A1-18
4   Register Bits S1-17; H staticiser
5   Register Bits J1-17; T staticiser
6   Register Bits M1-18
7   16 Control matrix steps and Timer Waveforms

8
9
10   4 times 18, control output waveforms
11   for computation and store access

(b)   A VOLUME CONTROL and LOUDSPEAKER are provided. The loudspeaker emits an audible indication that the computer is running; the pitch of the note is controlled by the rate at which jump instructions are obeyed by the processor.

2.7.6   Operation without Control and Monitor Unit

The processor will operate without the Control Unit connected, automatically obeying previously stored program, after power has been correctly applied to the system.

During the period of time from the instant of switch-on until all interlocks have cleared (indicating that power has been correctly applied) a 'Reset' Signal will be applied to the processor and transmitted over the store and peripheral interfaces.

2.8   INITIAL INSTRUCTIONS

These instructions form a fixed program which is permanently available as a means of loading programs into the store using paper tape as the input medium.

The instructions are brought into use by the JUMP control; when in use they occupy locations 8180 to 8191 of the store. They operate on program level 1; once a program has been loaded and a 15 7168 or 7176 instruction obeyed the locations become available for normal use. For full details see Appendix A.

2.9   PAPER TAPE INPUT

The tape reader is a photo-electric mechanism operating at 250 or 500 characters per second. It is connected to a special 8-bit interface by means of a paper tape and teleprinter control unit which contains the instruction routing and control logic.

Characters are read from the paper tape into an 8-bit buffer register. The tape input instruction causes the contents of this buffer to be transferred into the A register. Eight track tape 1" wide is normally used but it is also possible to use five track (11/16") or seven track (7/8") tape.

To initiate reading from tape the READ button on the control panel must be pressed. This causes tape to be advanced until the leading edge of the next sprocket-hole is detected. At this point the clutch of the tape-reader is de-energised; the buffer is loaded and the tape stops. When a tape input instruction is obeyed the contents of the buffer are transferred to the Accumulator, the clutch is re-energised, the tape advanced to the next row and the buffer again loaded.

Controls for the paper tape reader are described in section 2.12. In addition two controls are mounted on the paper tape reader itself. These are:-

(a)   ON/OFF switch which switches the tape reader motor and lamp on or off as desired.

(b)   RUN OUT button which, when depressed, causes tape to be fed through the reader at full speed without being read. After use of this button the tape must be repositioned by use of the READ button.

If tape is not present in the reader, is removed or prevented from drawing through the reader, the reader STOP lamp is illuminated to indicate the error.

2.10   TELEPRINTER INPUT AND OUTPUT

2.10.1   General

A teleprinter, comprising keyboard, page printer, tape reader and tape punch, may be added to the standard 905 system via the paper tape and teleprinter controller. Speed of operation of the printer, reader and punch is 10 ch/s; the teleprinter can be used both for input and output, all inputs are recorded by the page printer or tape punch. The teleprinter operates on an 8-level code, details of which are given in Appendix B.

2. 10. 2   Mode of Operation

Input from the teleprinter utilizes the 15 2052 instruction; the effect of this is to shift the accumulator contents 7 places left and to logically mix the 8-bit character into the eight least significant digit positions of the accumulator.

Output to the teleprinter uses the 15 6148 instruction, this transfers the eight least significant bits of the accumulator to the teleprinter which prints and/or punches the appropriate character.

The control circuits incorporate a single 8-bit buffer, used for input and output.   The buffer may at any time be empty, busy, or full.

If a key is struck when the buffer is empty, the buffer will become busy, and the character is transmitted and printed.   The buffer will then become full.   An input instruction from the processor may now read the character and restore the empty state.

If a key is struck when the buffer is not empty, the character generated will be ignored, and consequently will not appear on the print-out.   The input channel will then be disabled until a gap of 200 milliseconds occurs between successive attempts to input.   This ensures that if a character read from the printer reader is missed, this cannot be overlooked.

When the buffer is not busy, an output instruction from the processor may be obeyed.   The character will be accepted and the buffer will become busy until it has been printed.

If the buffer was full, or in process or receiving a character from the processor, then a character input from the keyboard will be lost.

Computer instructions may be held up in certain cases.

An output instruction issued when the buffer is busy will be held up until the transmission currently in progress is complete.   This may be the output of the previous character, or the acceptance of a character from the keyboard.

An input instruction, issued when the buffer is not full, will be held up until the buffer is full; i. e. until a key is struck and the character is received by the buffer register.

2.11   PAPER TAPE OUTPUT

2.11.1   General

A paper tape punch, operating at maximum speed of 110 ch/s with necessary control circuits, can be added to the system via the paper tape and teleprinter controller.
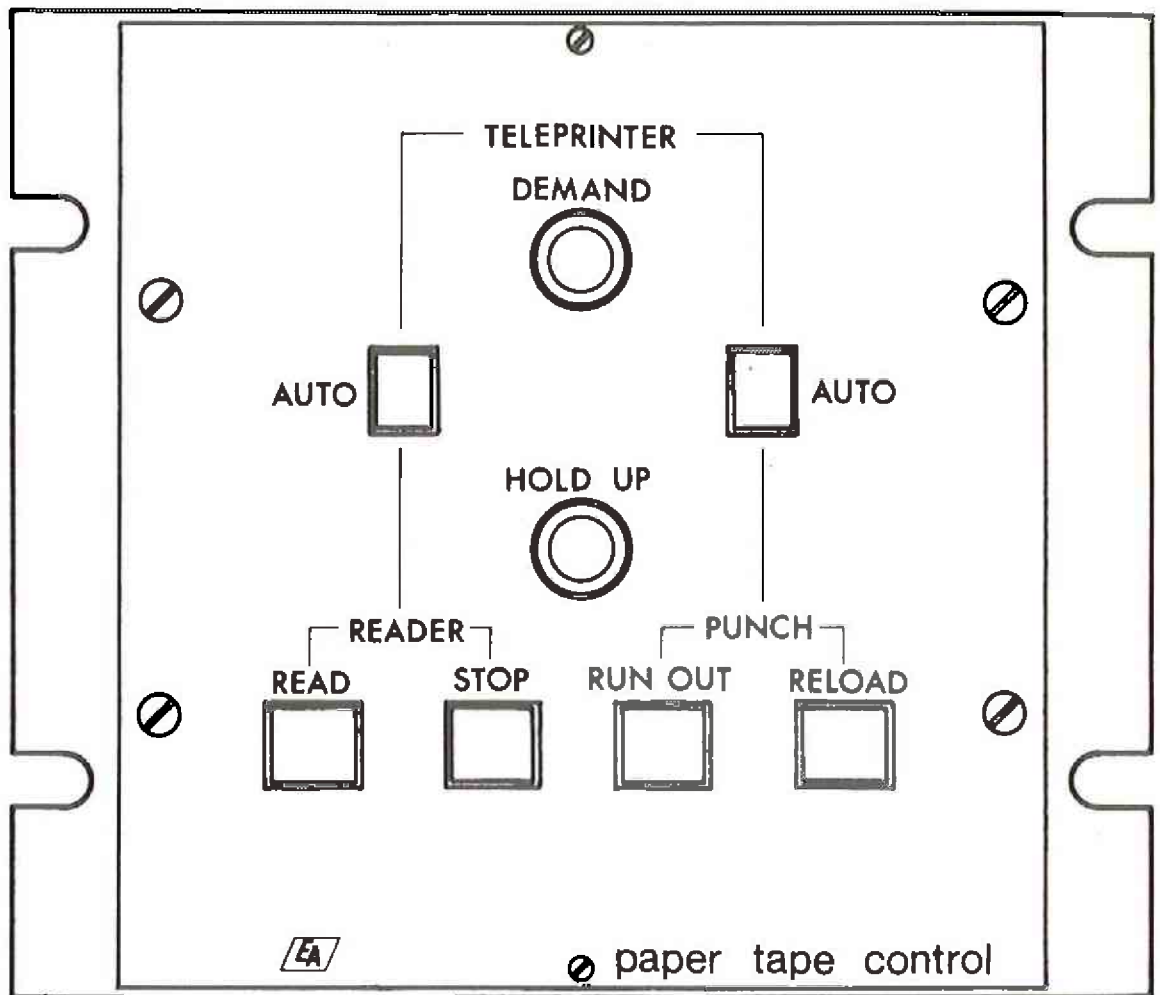
2.11.2   Mode of Operation

Output to the tape punch utilizes the instruction 15 6144; this sends the eight least significant bits of the accumulator to the tape punch control where they are held in a buffer register until the corresponding tape row has been punched. If five or seven track tape is used then the bits corresponding to the absent tracks must be zeros.

The punch motor will be switched off if no punch instruction is obeyed within approximately four seconds of the previous row being punched. Should the motor be off when a punch tape instruction is obeyed, the instruction will be completed immediately but punching will not take place for one second while the tape punch motor restarts.

2.12   PAPER TAPE & TELEPRINTER CONTROL PANEL (see Fig. 3)

(a)   Tape reader controls. These operate in any position of the master switch and are as follows:-

(i)   The READ push button is used to position the tape correctly in the reader after loading, and to resume reading after the tape has been stopped. The READ lamp, incorporated in the push button, is illuminated when the tape reader has been loaded until the button has been pressed.

(ii)   The STOP push button causes the tape reader to stop. The STOP lamp, incorporated in the push button indicates when this has been done.

TELEPRINTER

DEMAND

AUTO

AUTO

HOLD UP

READER

READ   STOP

PUNCH

RUN OUT   RELOAD

EA   paper tape control

PAPER TAPE AND TELEPRINTER CONTROL PANEL   Fig. 3

(iii)   The HOLD UP lamp which indicates when the computer is held up by the tape reader, or by the optional tape punch or teleprinter.

(iv)   The SELECT INPUT switch enables input instructions to be diverted between the tape reader and the teleprinter as follows:-

Switch position	Effect of input instructions	
	15 2048	15 2052
READER	Reader input	Reader input
AUTO	Reader input	Teleprinter input
TELEPRINTER	Teleprinter input	Teleprinter input

(b)   Teleprinter controls and indicators

The DEMAND lamp is lit when the computer is held up waiting for input from the teleprinter.

The teleprinter ON-LINE switch controls whether the teleprinter is available for program operation or for off-line use.

(c)   Tape punch controls and indicators

(i)   RUN OUT button. This causes blank tape to be fed from the punch.

(ii)   RELOAD lamp and push button. This lamp is lit when the "low tape" contacts on the tape operate; it remains lit, and further punch tape instructions will be held up, until a new tape reel has been loaded and the RELOAD push button operated.

(iii)   The SELECT OUTPUT switch enables output instructions to be diverted between the tape punch and teleprinter as follows:-

Switch position	Effect of output instructions	
	15 6144	15 6148
TELEPRINTER	Teleprinter output	Teleprinter output
AUTO	Punch output	Teleprinter output
PUNCH	Punch output	Punch output

2.13 ON-LINE PROGRAM FACILITY

2.13.1 Introduction

The "On-line Program Facility" allows the tape reader, tape punch and teleprinter to be operated in either an "on line" or "off line" mode. The mode of operation is determined by program control.

When operating in an "off line" mode the processor is held up until the device required is ready. In the "on line" mode, the processor will not be held up for more than 2μs whatever the state of the device required.

An instruction is available to input a status word from the paper tape station (PTS) to determine whether the selected devices are ready. A further instruction will output a control word to put the PTS "on line" or "off line". In the "on line" mode, if a device is addressed when it is busy the characters input to the processor are undefined and any characters output (including the character which caused the device to become busy) may be corrupted or lost.

Status signals, indicating at all times the states of the selected devices, are available at outlet sockets of the PTS.

2.13.2 Modes of Operation

2.13.2.1 The following operations can be performed with the "on line" adaptor facility.

(a)   Input a status word to the processor to indicate the availability of devices.

(b)   Output a control word from the processor to set the PTS either "on line" or "off line".

2.13.2.2   The instruction to input a status word from the PTS will be:-

15   2049

The status word shall have the following meaning -

Bit one set   - Reader buffer loaded.
Bit two set   - Punch ready.
Bit three set - Teleprinter input buffer loaded.
Bit four set   - Teleprinter output ready.

N.B. The bits of the status word will only indicate the state of the selected device. When the SELECT INPUT or SELECT OUTPUT switches are set to AUTO, the status word indicates the state of the program selected device. When these switches are set to a position other than AUTO, the status word indicates the state of the operator selected device e.g. if punch output is selected by the program, and this has been overridden by the operator selecting teleprinter output then bits 2 and 4 of the status word will indicate whether the teleprinter is ready.

2.13.2.3   The instruction to output a control word to the PTS will be:-

15   6145

The control word shall have the following meaning:-

Bit one set to "1" - Set the PTS to "on line" mode.
Bit one set to "0" - Set the PTS to "off line" mode.

2.13.2.4   Four status signals, corresponding to the four bits of the status word, are available on a separate interface. They may be used, for example, as inputs to an interrupt scanner.

2.13.3   Notes on Use

The status signals and bits of the status word are set to the "1" state when the appropriate device is ready to accept an instruction as detailed above. They will return to the "0" state as the instruction is obeyed. They may also return to the "0"

state as a result of operator intervention or other events as follows:-

Tape reader ready - this will return to "0" if the reader is unloaded, the "stop" or "run-out" buttons pressed or tape "creep" is detected.

Tape punch ready - this will return to "0" if the "run-out" push-button is operated or the tape reel is removed from the punch.

Teleprinter input ready - this will return to "0" if teleprinter output instruction is obeyed, as the teleprinter buffer register is used for both input and output.

Teleprinter output ready - this will return to "0" if a character is received from the teleprinter (as a result of a key being depressed or the teleprinter reader started) to load the buffer; it remains in this state while the buffer is busy (i.e. for the 100ms required to load it) but returns to "1" when the buffer is full as an output instruction can then be obeyed.

Any allocation of device selection by the operator will result in a corresponding change in the ready indicators.

2.14   PERIPHERAL INTERFACE

2.14.1   General

The 905 Standard Peripheral Interface has 59 signal lines used as follows:-

DATA OUT, 18 lines, used to transfer complete 18-bit words from the computer to the peripheral.

DATA IN, 18 signal lines, used to transfer complete 18 bit words from the peripheral to the computer.

ADDRESS, 11 signal lines, these carry the less significant binary digits of the address part of the input or output instructions. They select a peripheral and detail the operations to be performed.

SELECT, two signal lines, these specify
input or output transfer and are set by
the central processor as specified by bit
13 of the instruction address.

INTERRUPT, three signal lines, used by
the peripheral to interrupt the computer
on a priority system.

REPLY, used by the peripheral to
indicate when the data lines have been
served.

BLOCK TRANSFER and LAST WORD,
signals from the computer associated
with input/output transfers.

Miscellaneous, four signal lines.

2.14.2   Transfers

Two types of transfer are provided for:

(a)   Single word; one 18-bit word is trans-
            ferred by a single instruction (Function
            15, address range 0 to 6159) to or from
            the accumulator register.

(b)   Block transfer; a series of 18-bit words
            is transferred by a single instruction
            (Function 14, address range 2048 to 6143)
            to or from a series of consecutive store
            locations.   The first store location used
            and the number of words to be trans-
            ferred are programmed into the A and Q
            registers respectively prior to the block
            transfer instruction.   The contents of Q
            are integers within the range 0 to 4095.

2.14.3   Interface Signal Lines

2.14.3.1   General

All interface lines carry
binary signals, the states of these are described as 1 or 0 if the line
carries a digit of a binary number and as true or false if the signal
has a logic function.

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2.14.3.2 DATA IN lines

There are 18 DATA IN lines. These carry complete 18-bit words transferred from the peripheral to the accumulator by input instructions. The peripheral must place data on the DATA IN lines only when ADDRESS, in conjunction with INPUT SELECT or BLOCK TRANSFER, indicate that it is addressed by the current instruction. The DATA IN lines will be zero when the peripheral is not selected by the ADDRESS lines, also they will be zero when the peripheral sets REPLY true when INPUT SELECT is false (i.e. for an output function).

2.14.3.3 DATA OUT lines

There are 18 DATA OUT lines, these carry complete 18-bit words transferred from the accumulator to the peripheral by output instructions. They are significant only while OUTPUT SELECT is true. Their significance at all other times is undefined.

2.14.3.4 ADDRESS lines

There are 11 address lines, these carry bits 1 to 11 of the address part of the instruction and are used to select the peripheral device and to detail the operation to be performed.

The address lines are significant only while OUTPUT SELECT, INPUT SELECT or BLOCK TRANSFER is true. Their significance at all other times is undefined.

The central processor determines from the instruction function bits 17-14 and address bit 13 whether it is:

(a) an input or output instruction, or

(b) a single or block transfer, and

(c) from address bit 12 whether it is a peripheral or paper tape instruction.

Using this information the central processor sets true the relevant interface signals.

INPUT SELECT

This signal is set true by the central processor when an input transfer instruction is performed. The peripheral selected by the instruction address bits 1-11 places a word on the DATA IN lines when this line is set true. Having done this the peripheral sets true the REPLY line to the central processor.

INPUT SELECT is set false by the central processor when it has received REPLY true and has read the DATA IN lines. It remains false at all other times.

OUTPUT SELECT

This signal is set true by the central processor when an output transfer instruction is performed. The peripheral selected by the instruction address bits 1-11 will read the word on the DATA OUT lines and then set true the REPLY line to the central processor.

OUTPUT SELECT is set false by the central processor when it receives REPLY true. It remains false at all other times.

REPLY

This signal to the central processor is set true by the peripheral when:-

(a)   For an input transfer, the peripheral has placed a word on the DATA IN lines. The central processor will not read the DATA IN lines until REPLY is set true.

(b)   For an output transfer, the peripheral has read the word on the DATA OUT lines.

In both cases the central processor will stop, with the relevant SELECT signal true, until the peripheral sets REPLY true.

REPLY is set false by the peripheral as soon as possible after the SELECT signal becomes false and remains so at all other times.

The peripheral can only set REPLY true if the ADDRESS lines indicate that it is the particular device addressed by the current instruction.

BLOCK TRANSFER

This signal is set true by the central processor to indicate the commencement of a block transfer operation. It is set true before the relevant SELECT signal is set true for the first transfer. It remains true until the end of a block transfer, i.e. until after SELECT has become false after the LAST WORD transfer.

LAST WORD

This signal is set true by the central processor when the last word of a block transfer is being transferred. It is true for the duration of the relevant SELECT signal for this transfer, and false while SELECT is true for all other transfers in the block transfer.

Its significance when SELECT is false and for a single transfer is undefined.

INTERRUPTS

There are three INTERRUPT lines from the peripheral to the central processor; they are INTERRUPT 1, INTERRUPT 2, and INTERRUPT 3. One (or more) is made true when the peripheral requires the central processor to enter the program at that level (1, 2 or 3 respectively), the higher priority program being entered if more than one level of INTERRUPT is given. The relevant INTERRUPT line must be held true for at least 15μs and should be made false before the termination of the entered program. If it is not made false the program will be re-entered.

RESET

This line from the central processor carries the logic signal RESET, which becomes true when the computer is switched on, and if operating in the AUTO mode will become false when the power supply lines are established. In MANUAL or TEST modes the line is made true on switching on or after operating the RESET control until the JUMP control is operated. The line will normally be false but will become true when switching off or if any power supply line or store temperature fault occurs. The signal may be used to reset the peripheral device to its initial state.

POWER ON

This line is energised when power is applied to the central processor logical circuitry and de-energised when power is removed.

MAINS INTERRUPT

This line is set false when the computer is switched on and will become true at least 100µs before RESET is made true during switch off or because of mains failure. It can be linked directly to an interrupt line to enable any mains failure program to store the register contents which would otherwise be lost.

AUTO

This line is true in the 'AUTO' mode and false in the 'MANUAL' or 'TEST' modes.

2.14.4   Equipment Design: Timing Requirements

These timing requirements do not refer to any particular 900 series computer or peripheral: they are limiting design requirements which all 900 series peripherals and computers must meet. In the case of synchronously operated devices, which will fail if a response is not received within a limited time, the performance of the particular computer concerned must also be considered, as a minimum data transfer rate is not specified or implied.

Equipment should be designed to meet these requirements and to work satisfactorily with other equipment designed to meet these requirements.

2.14.4.1   Single word input (see Figure 4).

(a)   Computer

The ADDRESS signals must be in the correct state at least 200ns before INPUT SELECT is set true and must remain correct until 200ns after INPUT SELECT has become false.

The DATA IN signals must not be assumed to be correct until at least 500ns after REPLY becomes true; INPUT SELECT must not be set false until the DATA IN signals have been staticized within the computer.

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INPUT SELECT must not be set
true until at least 200ns after
REPLY has returned to FALSE.

(b)   Peripheral

REPLY must not be set true
until the DATA IN signals have
been set correctly. DATA IN
must be set ZERO by the time
REPLY is set false.

2.14.4.2   Single word output (see Fig. 5)

(a)   Computer

The ADDRESS and DATA OUT
signals must be in the correct
state at least 200ns before
OUTPUT SELECT is set true and
must remain correct until at least
200ns after OUTPUT SELECT is
set false again. The latter event
must not occur until at least 500ns
after REPLY has become true.

OUTPUT SELECT must not be
set true until at least 200ns
after REPLY has become false.

2.14.4.3   Block input (see Fig. 6)

(a)   Computer

The ADDRESS signals must be
in the correct state at least
200ns before BLOCK TRANSFER
is set true and must remain correct
until at least 200ns after BLOCK
TRANSFER is set false.

BLOCK TRANSFER must be
true at least 200ns before
INPUT SELECT is set true

for the first word and must
remain true until at least 200ns
after INPUT SELECT is set
false after the last word transfer.

The DATA IN signals must not
be assumed to be correct until
at least 500ns after REPLY
becomes true.

INPUT SELECT must not be
again set true until at least
200ns after REPLY has
returned false.

The LAST WORD signal must
be again set true until at least
200ns after REPLY has returned
false.

The LAST WORD signal must
be correct at least 200ns
before INPUT SELECT goes
true and must remain correct
until at least 200ns after INPUT
SELECT becomes false again.

(b)   Peripheral

REPLY must not be set true
until the DATA IN signals have
been set correctly.

DATA IN lines must be set to
zero not more than 200ns
after BLOCK TRANSFER
has been set false.

2.14.4.4   Block output (see Fig. 7)

(a)   Computer

The ADDRESS signals must be
in the correct state at least
200ns before BLOCK TRANSFER
is set true and must remain

900 SERIES INTERFACE SINGLE WORD INPUT TIMING   Fig. 4
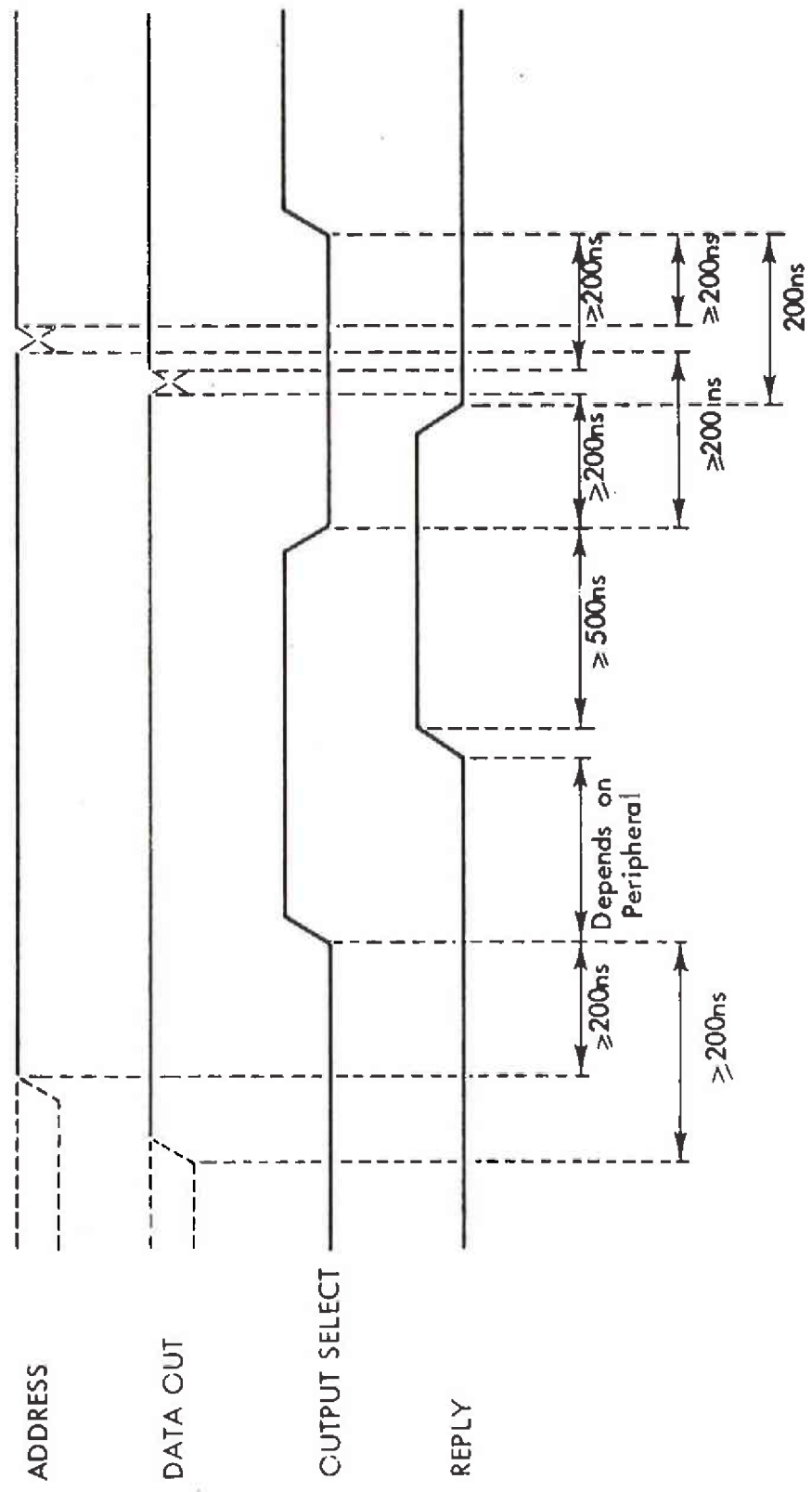
Fig.5   900 SERIES INTERFACE SINGLE WORD OUTPUT TIMING
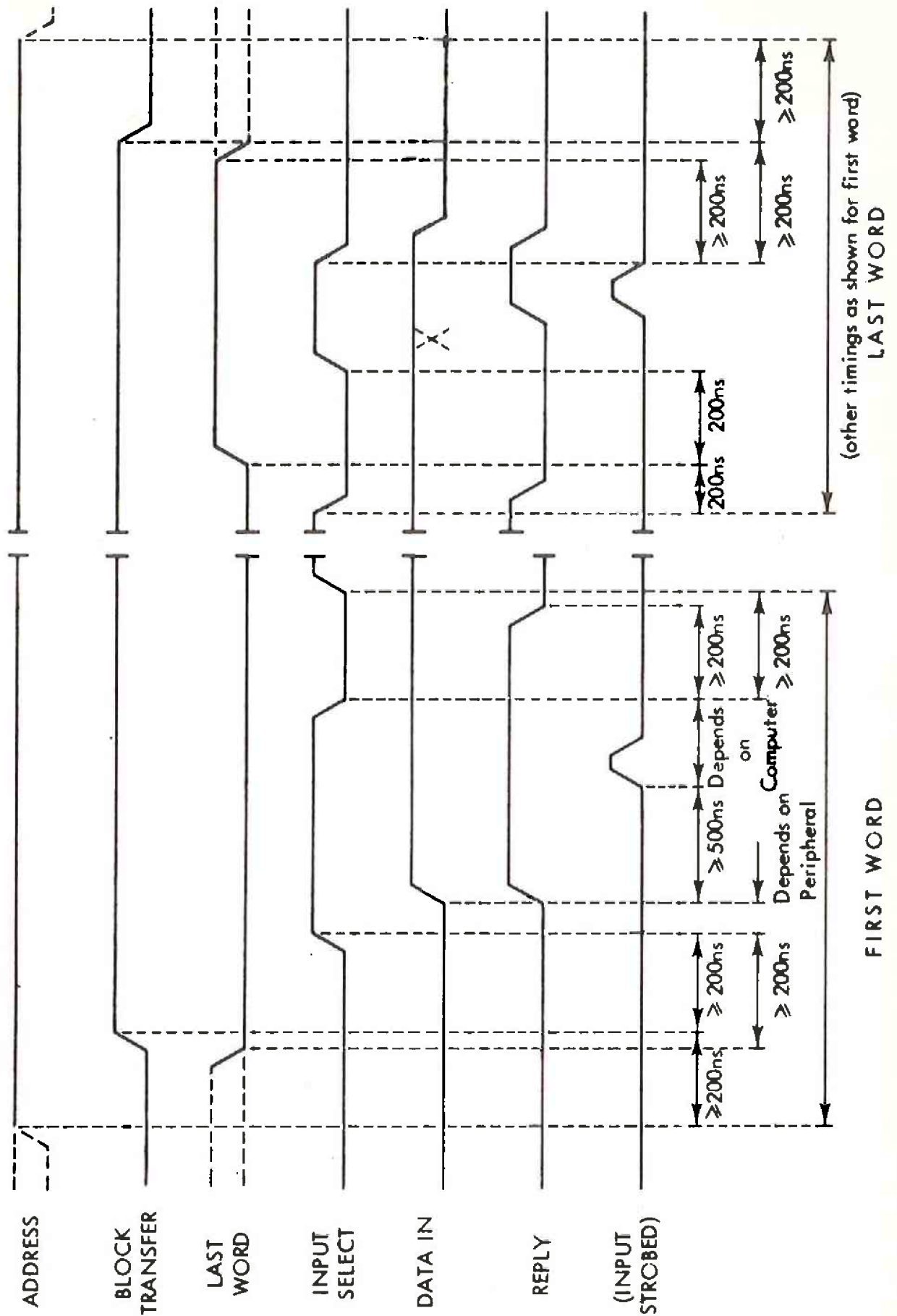
900 SERIES INTERFACE BLOCK INPUT TIMING

Fig. 6

39
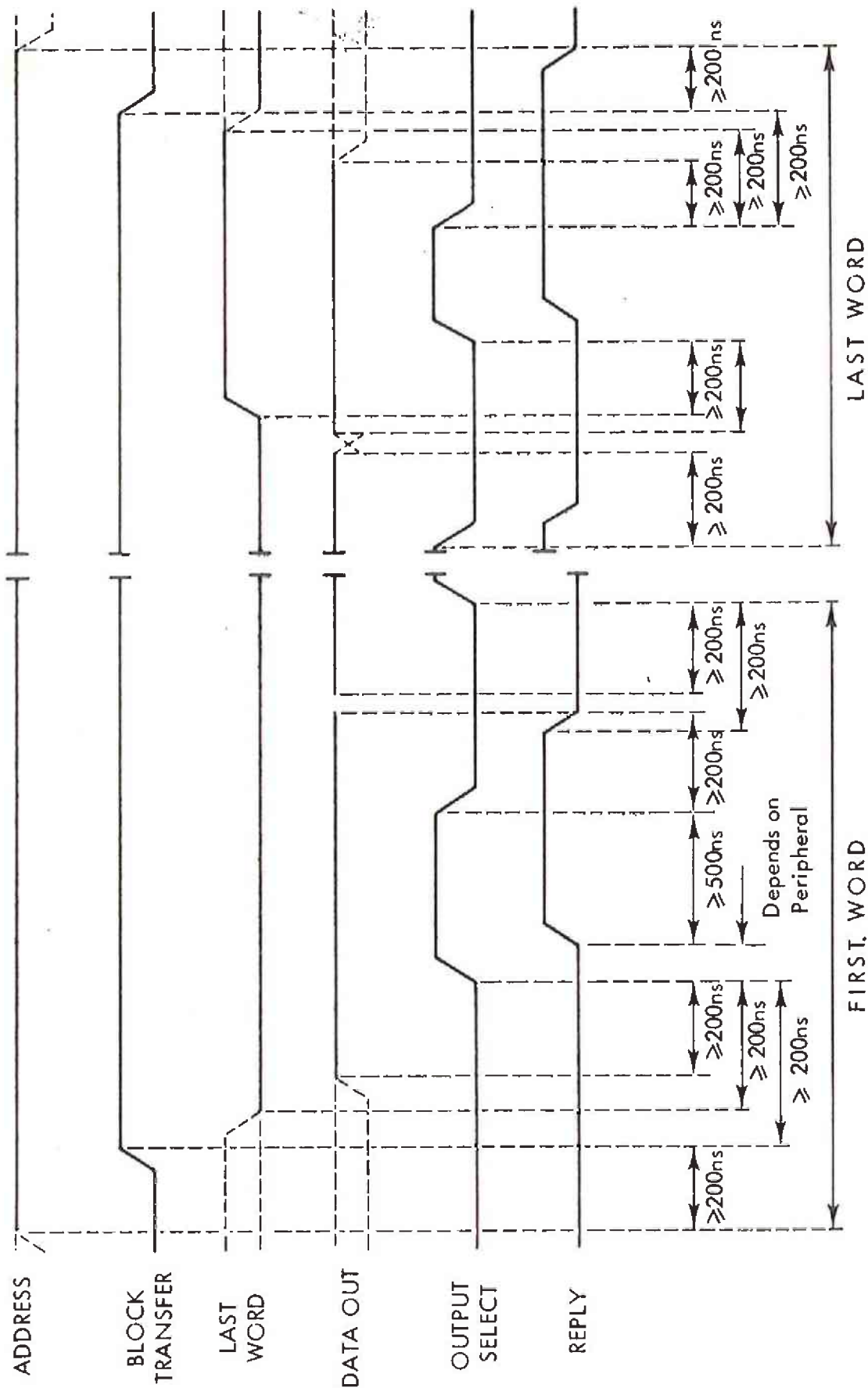
Fig. 7   900 SERIES INTERFACE BLOCK OUTPUT TIMING

correct until at least 200ns
after BLOCK TRANSFER is
set false.

OUTPUT SELECT must not be
set true for the first word until
at least 200ns after BLOCK
TRANSFER has been made true;
BLOCK TRANSFER must not be
set false until at least 200ns after
OUTPUT SELECT has been set
false for the last time.

The DATA OUT lines must be
correct at least 200ns before
OUTPUT SELECT is set true
and must remain correct until
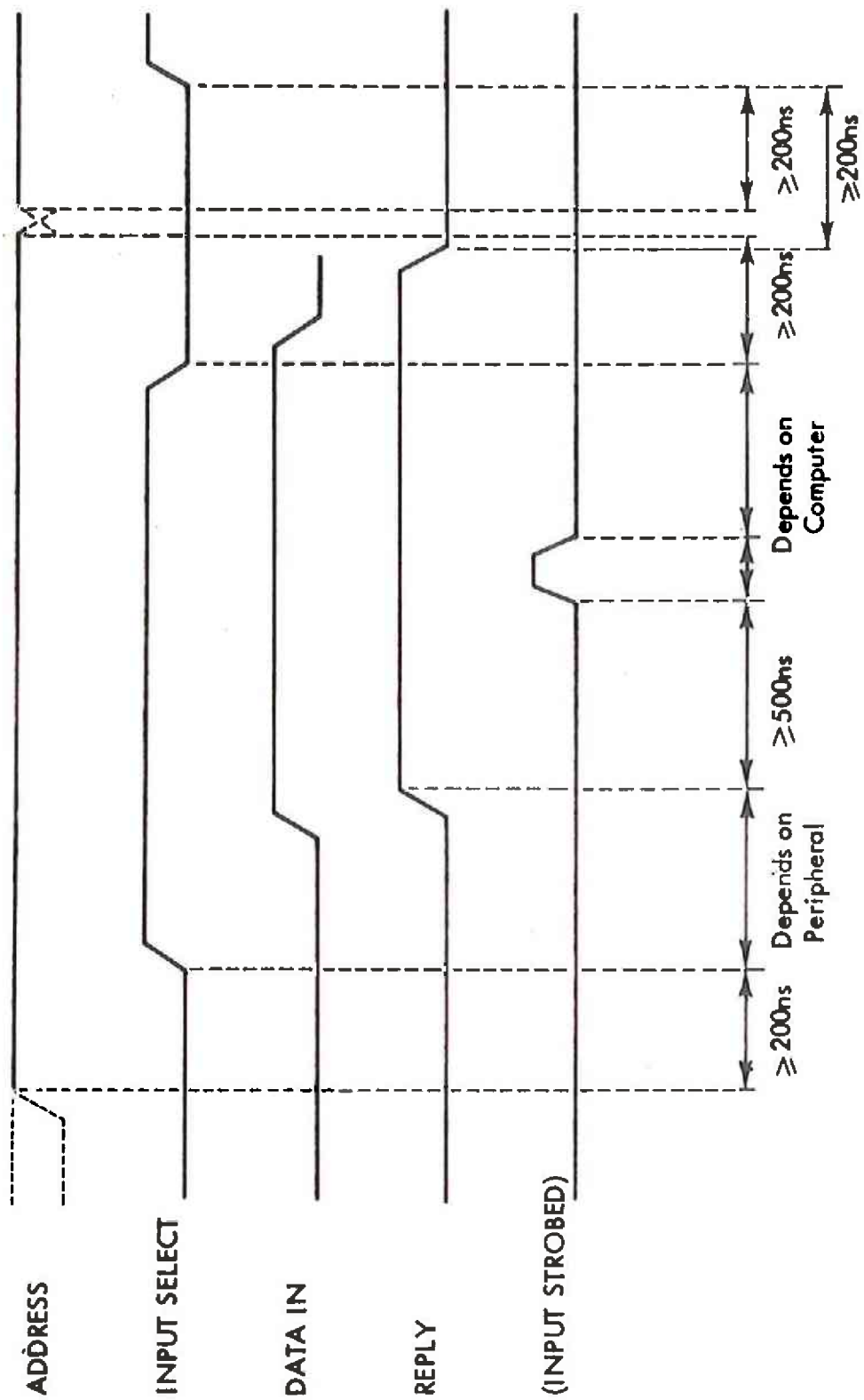at least 200ns after OUTPUT
SELECT has been set false again.

OUTPUT SELECT must not be set
false until at least 500ns after
REPLY has become true, and
must not be set true again until
at least 200ns after REPLY has
returned to false.

The LAST WORD signal must be
correct at least 200ns before
OUTPUT SELECT is set true.

2.14.4.5   Equipment design: address
conventions

The following conventions in
the use of the address lines should be observed.

Address lines 7 to 11 are used
to define the device (or in some cases the group of devices) to be selected.
A unique combination of these digits (which, interpreted as a binary
integer, is referred to as the "class number") must be assigned to each
peripheral.   A list of class assignments for standard peripherals and
recommendations is available on request.

Address lines 1 and 2 are
used to define the type of instruction as follows:-

Operation	Address 1	Address 2	Type
OUTPUT	0	0	Data output
	1	0	Control output
	0	1	Data Terminate
INPUT	0	0	Data input
	1	0	Status input

The control output type of instruction outputs a control word (or words) to the peripheral. The control word defines the action required of a peripheral; this action may involve the transfer of data words to or from it by means of data input or data output types of instruction. The Data Terminate instruction is used to signal the end of a series of data inputs or data outputs to the peripheral if this is required. (This duplicates the effect of the 'last word' indication during block transfers). The status input type instruction is used when it is required to determine the state of a peripheral device (e.g. busy indication, error indication, etc.).

Address lines 3 to 7 are generally not used. In some circumstances it may be necessary to use these to further define the peripheral action. Preferably, this should be done by means of a control word whenever possible.

2.14.5   Interface Circuits

Signal levels are:

	"0" or False	"1" or True
Transmitter	< 0.4 V	> 3.2 V
Receiver	< 1.7 V	> 2.6 V

The circuits of the transmitters and receivers used for all peripheral interface signals except "Power ON" are shown on Elliott drawings 322 MSA 3677, sheets 1 and 2, obtainable from MCD on request.

The circuits recommended for use in peripherals are:-

(a)   Circuitry as used in the computer
       (sheet 1):

       Four peripheral receiver circuits
       of this type may be connected in
       busbar fashion to one computer
       transmitter circuit. One peripheral
       transmitter circuit can be connected
       to one computer receiver circuit,
       i.e. a "fan-out" of four is permissible
       but "fan-in" is limited to one.

(b)   Alternative circuitry as shown on
       sheet 2:

       With these circuits "fan-out" and
       "fan-in" are both limited to one.

2.14.6 Cable Screening

"Data out", "data in" and "address"
signals must be carried in multi-way overall screened cable. Other
signals must be carried in coaxial cables (50 ohm). It is recommended
that all cable screens be connected to signal earth (0V) at both ends and
that this should be done as near as possible to the transmitter or
receiver circuit 0V connections.

When coaxial cables are taken through
a plug and socket other than a coaxial one, a separate way should be
used for each screen connection, which should be adjacent to the
corresponding signal way. Screens should not be bonded other than by
the connections to 0V.

The maximum recommended cable
length is 20 ft.

2.15   POWER SUPPLIES

2.15.1 Mains Supply

The basic 905 system requires an a.c.
mains supply as follows:-

Voltage:	200/210/220/230/240/250 selected by tapping
Frequency:	50Hz
Tolerances:	Voltage ± 10%
	Frequency ± 1Hz (45Hz to 440Hz when paper tape and tele-printer not used).

2.15.2 Power Consumption

Current consumption of the standard 905 system complete with tape reader, punch and teleprinter, is 1.7kVA with 2μs store, 1.9kVA with 1μs store.

2.15.3 Interference

The system incorporates radio-frequency filters in series with the incoming mains supply. These give suppression of > 60dB over the range 150kHz to 20MHz and treater than 40dB over the range 20MHz to 150MHz.

2.15.4 Protection

The incoming mains supply is fused at 10A.

The supplies to the various circuits are individually fused and current-limited; high speed over-voltage protection is also fitted.

2.15.5 Failure

In the event of failure of the supply for a period exceeding 10ms (and on switching off) the computer will revert to the RESET state and the power supply will be switched off in such a way as to retain store contents. When the mains supply is resumed, the computer will start obeying program automatically if the MASTER SWITCH is in the AUTO mode; in the MANUAL or TEST modes it will remain reset until the JUMP control is operated. The register contents will be lost unless use is made of the MAINS INTERRUPT signal.

2.16 INSTALLATION

2.16.1 Dimensions

A 905 system consists basically of a series of 19in rack-mounting units requiring an overall depth of $22\frac{3}{4}$in. Dimensions of these units are as follows:-

(a)   System with 2μs store

Unit	Height	Approx. Weight
Processor	$10\frac{1}{2}$in	25lb
Store	$5\frac{1}{4}$in	20lb
Power supply, Type 2	7in	40lb
Power supply, Type 3	7in	40lb

Unit	Height	Approx. Weight
Cooling fan	$3\frac{1}{2}$in	7lb
Control & monitor panel	7in	10lb
Paper tape control logic & PSU	$19\frac{1}{4}$in	88lb
Paper tape control panel	$1\frac{3}{4}$in	3.5lb

(b)   System with 1μs store

Unit	Height	Approx. Weight
Processor	$10\frac{1}{2}$in	25lb
Store	7in	25lb
Power supply, Type 1	7in	40lb
Power supply, Type 3	7in	40lb
Cooling fan	$3\frac{1}{2}$in	7lb
Control & monitor panel	7in	10lb
Paper tape control logic & PSU	$19\frac{1}{4}$in	88lb
Paper tape control panel	$1\frac{3}{4}$in	3.5lb

The tape reader is a free standing unit, additional to the above; it is 6.2in wide, 10.5in deep and 10in high, weighing 17lb. A simple tape reel box for use with the tape reader is supplied.

The teleprinter is supplied complete with stand for floor mounting; it has the following dimensions:-

Height: 33in (8.4in without stand)   Depth: 18.5in
Width: 18.6in   Weight:60lb

The tape punch mechanism is mounted within a sound reducing enclosure with the following dimensions:-

Height: 13.75in   Depth: 19in
Width: 10in   Weight: 50lb

The 19in rack-mounting units may be supplied fitted in standard instrument cabinets, as shown in Fig. 8 or as a desk on which tape reader, punch and control panel are mounted (see Fig. 9).

NOTE: The relative positions of units as shown in these diagrams are recommended for all installations.

2.16.2 Environment

The 905 will operate at temperatures within the range 0°C to 40°C (the upper limit may be extended by a suitable cooling system). Humidity limits are 20 - 90% with no condensation (30 - 70% is recommended when paper tape is used).

2.16.3 Storage

The units of a 905 system may be stored without detriment at temperatures between -10°C and 60°C and humidity up to 95% RH (without paper tape). It is recommended that units be subjected to a functional test at annual intervals. Under these conditions the shelf life is not less than 5 years.

21"
(53cm)

CONTROL AND MONITOR
UNIT

STORE 1μs

SPACE FOR STORE

DEPTH 22¾"
(57.7cm)

CENTRAL
PROCESSOR

54½"
(138.5 cm)

POWER SUPPLY
UNIT
TYPE 3

FAN UNIT

POWER SUPPLY
UNIT
TYPE 1

DOORS REMOVED FOR CLARITY
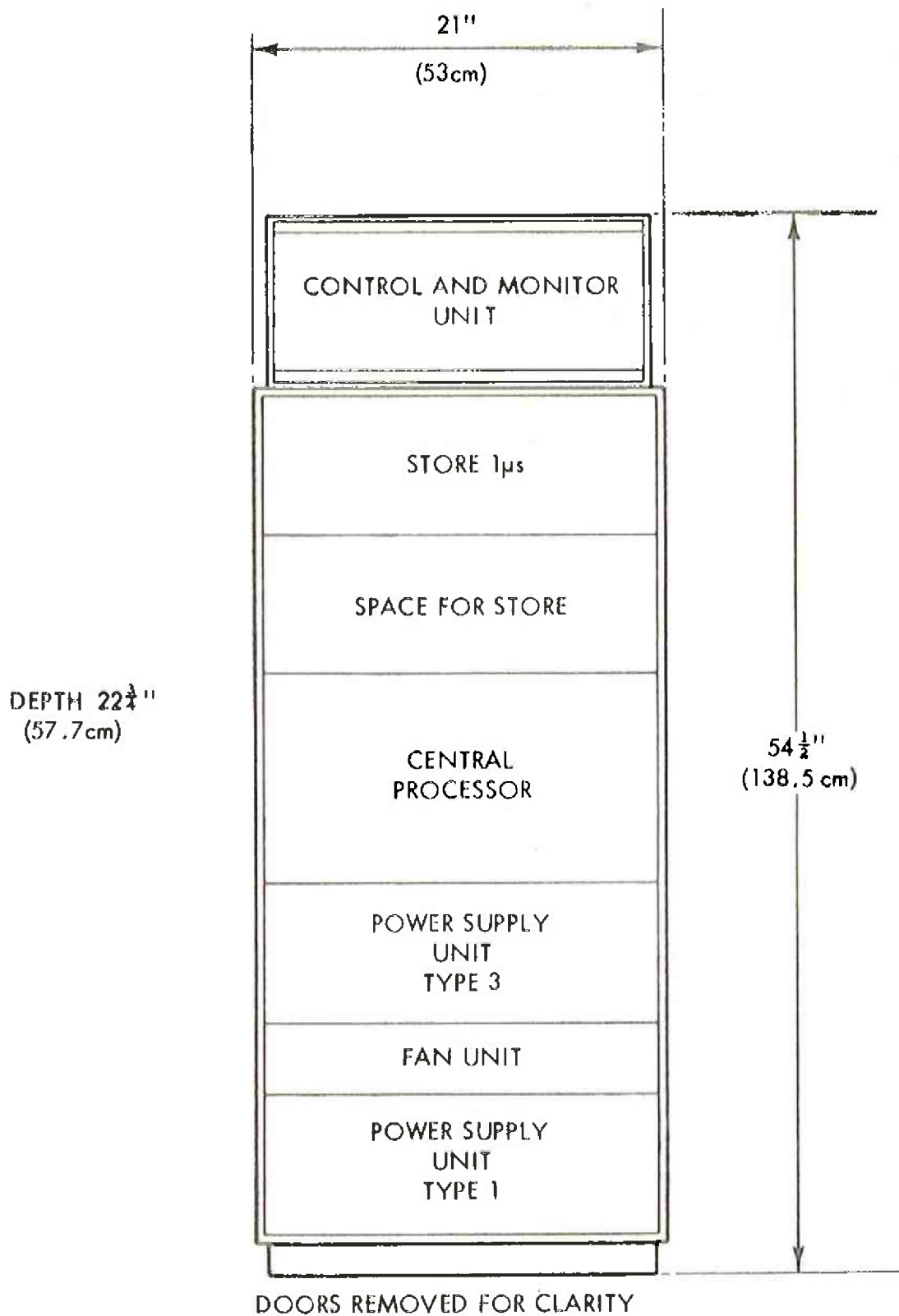
Fig. 8   DIMENSIONS, 905 STANDARD SYSTEM, 1μs STORE

PUNCH

READER

TAPE
DISPENSER

CONTROL AND MONITOR
UNIT

PAPER
TAPE
CONTROL

19 3⁄4 "
(50 cm)

SPACE

FAN UNIT

STORE 1μs

POWER SUPPLY UNIT
TYPE 1

SPACE FOR STORE

PAPER TAPE
LOGIC

CENTRAL
PROCESSOR

36"
(91·5 cm)

PAPER TAPE
POWER SUPPLY

POWER SUPPLY UNIT
TYPE 3

DOORS REMOVED FOR CLARITY

42" (107cm)

DEPTH 26" (66cm)
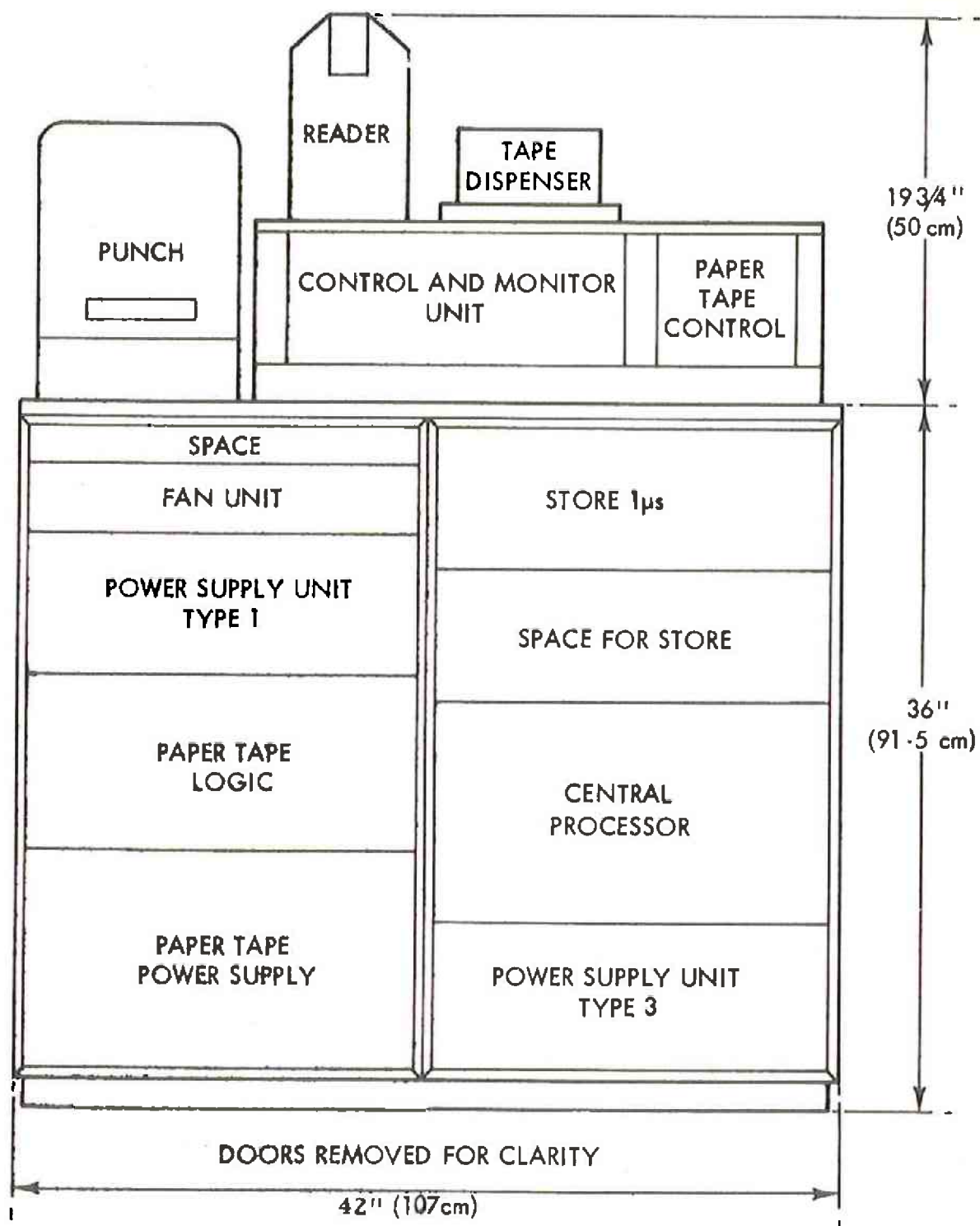
DIMENSIONS, 905 DESK-MOUNTED SYSTEM, 1μs STORE   Fig.9
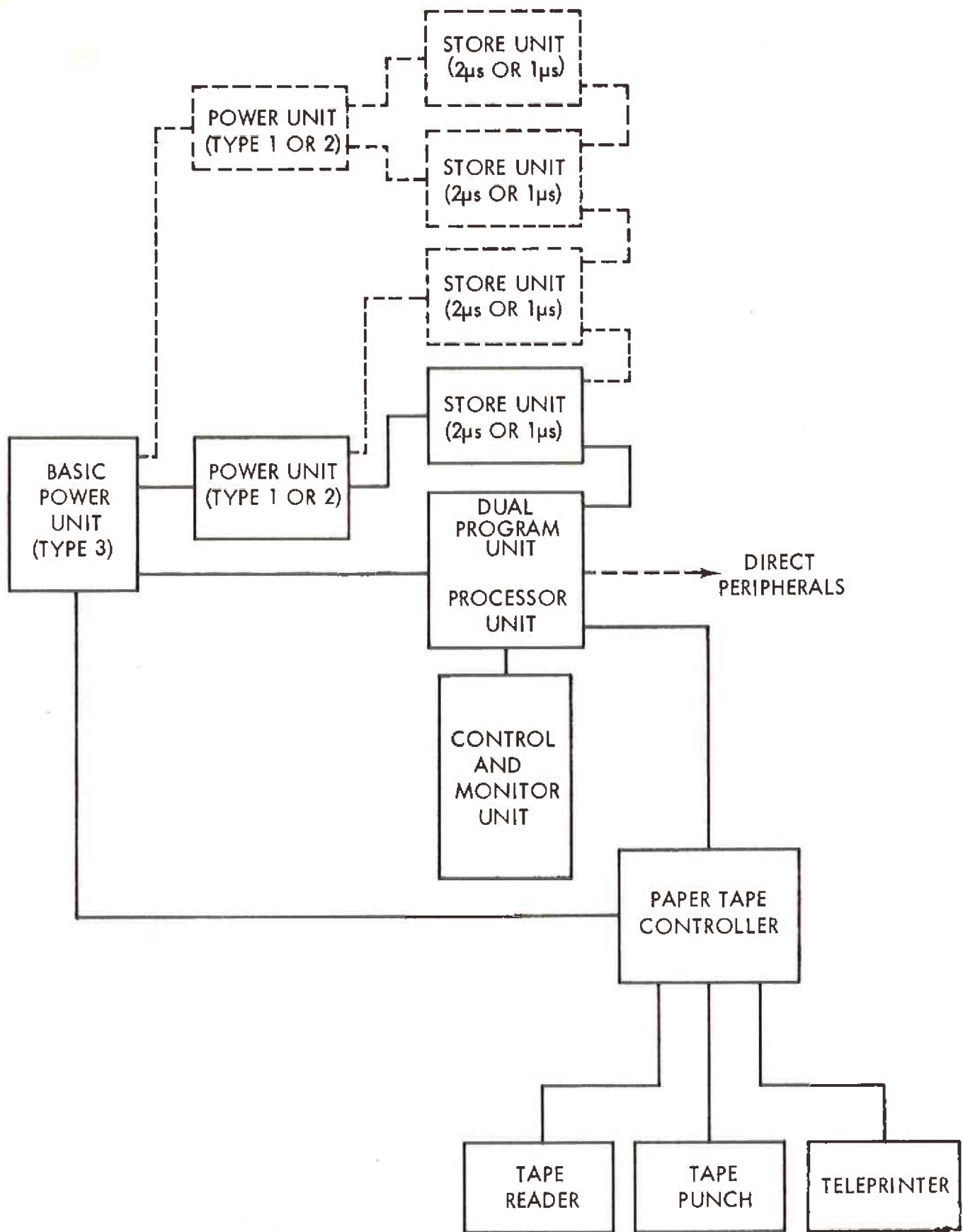
Fig. 10   BLOCK DIAGRAM-EXTENDED 905 SYSTEM

Chapter 3:   905 EXTENDED SYSTEMS

3. 1   STORE EXTENSION

3. 1. 1   Both the 1μs and 2μs stores may be extended from the standard 8192 words to a total of 65,536 words in units of 8192 words; provision is also made for future extension to 131,072 words in units of 16,384 words.

3. 1. 2   Instructions can be placed in any locations in the store; to allow this the S register, as stated in 2. 4, contains 17 bits thus allowing instructions to be extracted automatically from locations numbered 0 to 131,071.

3. 1. 3   Since the address part of an instruction is 13 digits in length, allowing a range of 0 to 8191, additional features are necessary to allow operand addresses in a store of more than 8192 words to be defined.

The actual address referred to by an instruction varies with the instruction type and the contents of the 1 bit Address Mode register (H) as follows:-

Instruction type	Store Address (unmodified)	
	H = 0	H = 1
Transfers between registers and store		
Arithmetic between registers and store	S |14-17| + N	N
Count in store		
Transfer control	S |14-17| + N	S |14-17| + N

The above can be summarised by saying that when H = 0 the N digits of an instruction specify the address of a location in the same unit as the instruction itself and when H = 1 the N digits specify an address in the first 8192 words (locations 0-8191) except for jump instructions which are as for H = 0.

In the case of modified instructions, the effect of modification is to add the B register contents to the address defined above; since the B register contains 18 bits a full-length address can always be generated and thus a modified instruction can always address any location in the store.

Functions 14 and 15, when N does not define a store location, are not affected by the contents of H and only the 13 least significant bits of a modified address are meaningful.

In the following tables the full range of operations available with extended store is listed:-

V is used to mean S [14-17] + N

3.1.4 Un-modified instructions (B = 0)

(a) Inter-register transfers

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
A to B	B: = A		{ 4.1	6.1	15	7174	Only valid when H = 1 or S [14-17] = 0
			3.3	5.3	5	M	
A to Aux.	Q [2-18] := A [1-17]		3.7	4.7	15	7172	Only valid when H = 1 or S [14-17] = 0
B to Q	Q: = B		3.6	6.6	0	M	
S to B	B [1-13] := S [1-13]	Q [14-17] := S [14-17]	3.3	5.3	11	M	
B to A	A: = B	B [14-18] : = 0	{ 4.1	6.1	15	7175	Only valid when H = 1 or S [14-17] = 0
		Q [1-13] : = 0	2.4	4.4	4	M	
Aux. to A	A [1-17] : = A [2-18]		3.7	4.7	15	7173	Only valid when H = 1 or S [14-17] = 0
Aux. to B			3.3	5.3	3	M	

(b) Transfers between registers and store (locations in same area as instruction)

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
Read	A: = V'		2.4	4.4	4	N	
Load B	B: = V'	Q: = V' No interrupt possible after this instruction	3.6	6.6	0	N	
Load O	O: = V'	B: = V' (No interrupt possible) (Or A: = V' -A)	3.6	6.6	0	N	
Write	V': = A		3.3	5.3	2	N	H=0
Store S	V' [1-13] := S [1-13] V' [14-17] := 0	Q [14-17] := S [14-17]	3.3	5.3	5	N	
Store Aux.	V' [1-17] := Q [2-18] V' [18]:= 0		3.3	5.3	3	N	

(c)   Transfers between registers and store (locations 0-8191)

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
Read	A:- N'		2.4	4.4	4	N	
Load B	B:- N'	Q:= N' (No interrupt after this instruction	3.6	6.6	0	N	
Load Q	Q:= N'	B:= N' No interrupt after this instruction OR A:= N' - A	3.6	6.6	0	N	
Write	N':= A		3.3	5.3	2	N	
Store	N' [1-13]:=S [1-13] N' [14-17] := 0	Q [14-17] := S [14-17]	3.3	5.3	5 / 11	N / N	H = 1 or S [14-17] = 0
Store Aux.	N' [1-17] := Q [2-18] N' [18] := 0		3.3	5.3	3	N	

(d)   Arithmetic between Accumulator and B register

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
Add A to BI	A:= A + B		2.4	4.4	1	M	
Subtract A from B	A:= B - A		3.3	5.3	2	M	H = 1 or S [14-17] = 0
Multiply A by B	AQ:= A x B	Q:= B	10.2	12.2	12	M	
Divide by B	A:= AQ ÷ B	Q [l] altered Q:= AQ ÷ B	19.3	21.3	13	M	
Collate A with B	A:= A and B		2.4	4.4	6	M	

(e) Arithmetic between Accumulator and store (locations in same area as instruction)

Name	Operation	Other effects	Time		Instruction		Notes
			1 μs store	2 μs store	F	N	
Add	A:= A + V'		2.4	4.4	1	N	
Negate and Add	A:= V' -A	Q:= V'	3.3	5.3	2	N	
Multiply	AQ:= A x V'	Q [1] altered	10.2	12.2	12	N	H = 0
Divide	A:= AQ ÷ V'	Q:= AQ ÷ V'	19.3	21.3	13	N	
Collate	A:= A and V'		2.4	4.4	6	N	

(f) Arithmetic between Accumulator and store (locations 0 to 8191)

Name	Operation	Other effects	Time		Instruction		Notes
			1 μs store	2 μs store	F	N	
Add	A:= A + N'		2.4	4.4	1	N	
Negate and Add	A:= N' - A	Q:= N'	3.3	5.3	2	N	H = 1 or
Multiply	AQ:= A x N'	Q [1] altered	10.2	12.2	12	N	S [14-17] = 0
Divide	A:= AQ ÷ N'	Q = AQ ÷ N'	19.3	21.3	13	N	
Collate	A:= A and N'		2.4	4.4	6	N	

(g) Transfer Control

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
Jump zero	if A = 0 then S:=V		1.2	2.2	7	N	
Jump	S:= V		1.2	2.2	8	N	
Jump negative	if A < 0 then S:= V		1.2	2.2	9	N	
Count and Test	B:= B+1 if B [1-13] = 0 then S:= S+2		5.3	8.3	15	7170	
Test standard	if A ≥ +$\frac{1}{2}$ or A< -$\frac{1}{2}$ or A=0 then S=S+2		6.2 / 2.9 / 3.8	9.2 / 4.9 / 5.8	15	7169	

(h) Miscellaneous

Name	Operation	Other effects	Time 1μs store	Time 2μs store	Instruction F	Instruction N	Notes
Count in B	B:= B+1		3.6	5.6	10	M	H=1 or S [14-17] = 0
Count in store	N':= N'+2^{-17}		3.6	5.6	10	N	H=1 or S [14-17] = 0
Count in store	V':= V'+2^{-17}		3.6	5.6	10	N	H = 0
Shift left	AQ:= AQ x 2^N		2.9+0.9n	3.9+0.9n	14	0to36	
Shift right	AQ:= AQ x 2^{N-8192}		2.9+0.9n	3.9+0.9n	14	8156to 8171	i.e. shift right 8192-N(=n) places
Terminate	Current program level terminated		7.4	11.4	15	7168	
Set relative	H:= 0		3.7	5.7	15	7176	Used only in conjunction with ex-tended store.
Set absolute	H: = 1		3.7	5.7	15	7177	

(i) Input and Output

Name	Operation	Other effects	Time		Instruction		Notes
			1μs store	2μs store	F	N	
Key input	A:= word generator		3.7	5.7	15	7171	Acc-shifted left 7 places and 8 bit character logically mixed in.
Tape input	A [9-18]:=A [2-11] A [8] := A [1] or character [8] A [1-7] := character [1-7]		5.5(min)	6.5	15	2048	
Teleprinter input	A [9-18]:= A [2-11] A [8] :=A [1] or character [8] A [1-7] := character [1-7]		5.5(min)	6.5	15	2052	- do - Input from tape reader when teleprinter not fitted.
Word input	A:= input word		5.5(min)	6.5min	15	0 to 2047	Input device and action selected externally by N [1-11]
Block input	A':= 1st input word (A+1)':= 2nd input word etc. (A+Q [1-12] -1)':= last input word	A, Q altered	3.8+ 5.5n (min)	4.8+ 6.5n min	15	2048 to 4095	input device and action selected externally by N[1-11] No. of words input =Q [1-12] (=n)
Tape output	Character:=A [1-8]		5.5(min)	6.5min	15	6144	
Teleprinter output	Character:=A [1-8]		5.5(min)	6.5min	15	6148	Output device and action selected externally by N[1-11] -do-
Word output	Output word:= A		5.5(min)	6.5min	15	4096	Output device and action selected externally by N[1-11]
Block output	1st output word:=A' 2nd output word:=(A+1)' etc. Last output word:= (A+Q [1-12] -1)'	A, Q altered	3.8+ 5.5n (min)	4.8+ 6.5n min	14	4096	No. of words output =Q [1-12]

3.1.5 Modified instructions

Modified instructions are not limited in respect of the store locations referred to. The modifier needed to refer to a particular location varies with the contents of H.

NOTE: X is used to mean B + N
Y is used to mean B + S [14-17] + N

Name	Operation	Other effects	Time 1 μs store	Time 2 μs store	Instruction F	Instruction N	Notes
Read	A:= X'	Q altered	3.6	6.6	4	N	H = 1 or S [14-17]
	A:= Y'	Q altered	3.6	6.6	4	N	= 0
Load B	B:= X'	Q:= X'	4.8	8.8	0	N	H = 1 or S [14-17]
	B:= Y'	Q:= Y'	4.8	8.8	0	N	= 0
Load Q	Q:= X'	{ B:= X', A:= X'-A }	4.5	7.5	2	N	H = 1 or S [14-17]
	Q:= Y'	{ B:= Y', A:= Y'-A }	4.8	8.8	0	N	= 0
Write	X':= A	Q altered	4.5	7.5	5	N	H = 1 or S [14-17]
	Y':= A	Q altered	4.5	7.5	5	N	= 0
Store S	X':= S [1-13]	Q:= S [14-17]	4.5	7.5	11	N	H = 1 or S [14-17]
	Y':= S [1-13]	Q:= S [14-17]	4.5	7.5	11	N	= 0

(b) Arithmetic between accumulator and store

Name	Operation	Other effects	Time		Instruction		Notes
			1 μs store	2 μs store	F	N	
Add	A: = A = X'	Q altered	3.6	6.6	1	N	H = 1 or S [14-17] = 0
	A: = A + Y'	Q altered	3.6	6.6	1	N	H = 0
Negate and add	A: = X' - A	Q: = X'	4.5	7.5	2	N	H = 1 or S [14-17] = 0
	A: = Y' - A	Q: = Y'	4.5	7.5	2	N	H = 0
Multiply	AQ: = A x X'	–	11.4	14.4	12	N	H = 1 or S [14-17] = 0
	AQ: = A x Y'	–	11.4	14.4	12	N	H = 0
Collate	A: = A and X'	Q altered	3.6	6.6	6	N	H = 1 or S [14-17] = 0
	A: = A and Y'	Q altered	3.6	6.6	6	N	H = 0

(c) Transfer Control

Name	Operation	Other effects	Time		Instruction	
			1 μs store	2 μs store	F	N
Jump zero	if A = 0 then S: = Y	Q altered	1.2 (A ≠ 0) 2.4 (A = 0)	2.2 (A ≠ 0) 4.4 (A = 0)	7	N
Jump	S: = Y	Q altered	2.4	4.4	8	N
Jump negative	if A< 0 then S: = Y	Q altered	1.2 (A≥ 0) 2.4 (A< 0)	2.2 (A≥ 0) 4.4 (A< 0)	9	N

(d) Miscellaneous

Name	Operation	Other effects	Time		Instruction		Notes
			1 µs store	2 µs store	F	N	
Count in store	$X' := X' + 2^{-17}$	Q altered	4.5	8.5	10	N	
Word input	A: = input word	Q altered	6.7 (min)	7.7 (min)	15	N	X in range 0-2047 device and action selected by X [1-11]
Word output	Output word:= A	Q altered	6.7 (min)	7.7 (min)	15	N	X in range 4096 - 6143, device and action selected by X [1-11]

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3.1.6 Program Compatability

The 905 with extended store can accept all programs written for 903 computers with extended store (as described in Volume 1 of the 903 Manual, Part 2, Sections 1 and 2 and Part 3 Section 4) if the H register contents are zero. For convenience of operating such programs the H register is automatically cleared when the Jump control is used. The appropriate version of the Symbolic Input Routine (SIR) and the ALGOL and FORTRAN compilers may thus be used.

3.2 MULTIPLEX INTERRUPT UNIT

3.2.1. The MIU allows up to seven peripheral devices to be multiplexed on to the direct interface outlet of the 905 and provides facilities for accepting and controlling up to 12 interrupt sources, grouped on to one program level, originating from the multiplexed peripherals or other external devices.

3.2.2 Peripheral Multiplexing

The unit is connected to the 905 direct interface outlet and provides up to seven outlets for the connection of peripherals. These outlets are in effect replicas of the processor direct outlet as regards signalling system, signal levels and physical details so that any peripheral may be used either on its own, connected directly to the processor or, in conjunction with others, connected via the MIU.

3.2.3 Interface Details

The signals available on each peripheral outlet are listed below, together with the corresponding signals of the processor interface.

Signals from the processor to peripherals are simply repeated by the MIU on each outlet where specified. Signals from peripherals (except interrupts and readies) are "OR-ed" together in the MIU and the resulting signal transmitted to the processor. The design requirements for peripheral signals are as stated for the processor interface in Section 2.14.3.

Central Processor	MIU	
	Outlet A	Outlets B-G
Data in 1-18	Data in 1-18	Data in 1-18
Data out 1-18	Data out 1-18	Data out 1-18
Address 1-2	Address 1-2	Address 1-2
Address 3-6	Address 3-6	-
Address 7-11	Address 7-11	Address 7-11
Input select	Input select	Input select
Output select	Output select	Output select
Reply	Reply	Reply
Block transfer	Block transfer	-
Last word	Last word	Last word
Interrupt 1	Ready X	-
Interrupt 2	Ready Y	Ready Y
Interrupt 3·	Ready Z	Ready Z
Reset	Reset	Reset
Power on	Power on	Power on
Auto	Auto	-
Mains failure	Mains failure	-

3.2.4   Interrupt Facilities

The M.I.U. contains facilities to allow up to 12 ready signals to be grouped via a 'masking' register, through an OR gate onto one of the central processor interrupts. In addition a further seven ready signals may be grouped through another OR gate onto a central processor interrupt line.

The mask register, on the first group of 12 ready lines, can be set by program to inhibit or enable any of the individual ready lines, and facilities are included to enable the program to determine the source of interrupt.

The program facilities take the form of the following instructions:-

Function	Instruction	
Read states of signal lines 1-12 into corresponding bits of the Accumulator (1 = ready, 0 = not ready)	15	64
Place number of highest priority signal causing interrupt into Accumulator. (Note: Priorities are assigned in numerical order, No. 1 having the highest priority and No. 12 the lowest. If no signals are present the Accumulator is cleared).	15	65
Set bits of mask register to the "one" state (i.e. allow interrupts from corresponding signals) if corresponding bits of Accumulator are "ones".	15	4160
Set bits of mask register to the "zero" state (i.e. inhibit interrupts from corresponding signals) if corresponding bits of Accumulator are "ones".	15	4161

Note that bits of the mask register in positions corresponding to zeros in the accumulator are not altered by the 15 4160 or 4161 instructions. The mask register is cleated when the computer is reset.

A program interrupt signal will be sent to the processor as a result of a signal on any of the 12 lines, provided that the corresponding mask register bit is set to "one". Use of the 15 65 instruction allows the processor to determine directly the source of the signal; signals which are "mask 1 off" do not affect the number read by this instruction. The 15 64 instruction, however, reads the actual state of all signals, irrespective of the mask register contents.

For systems using two MIU's the above instruction addresses are increased by two for control of the second unit.

3.2.5   Patching Facility

The interrupt signals to the processor, and the ready signals from the peripheral outlets, are all grouped on an additional connector; this enables the allocation of levels and priorities to be "patched" if necessary, and additional external signals connected where desired. The signals available on the connector, and the standard connections are as follows:-

From	To
Ready X Outlet A	**Interrupt 1 - Processor**
Ready Y Outlet A	
Ready Y Outlet B	
Ready Y Outlet C	
Ready Y Outlet D	OR inputs
Ready Y Outlet E	
Ready Y Outlet F	
Ready Y Outlet G	
OR output	Interrupt 2 - Processor
Ready Z Outlet A	Interrupt extension, signal 4
Ready Z Outlet B	Interrupt extension, signal 5
Ready Z Outlet C	Interrupt extension, signal 6
Ready Z Outlet D	Interrupt extension, signal 7
Ready Z Outlet E	Interrupt extension, signal 8
Ready Z Outlet F	Interrupt extension, signal 9
Ready Z Outlet G	Interrupt extension, signal 10
Interrupt extension output	Interrupt 3 - processor
Mains failure - processor	-
-	Interrupt extension, signal 1
-	Interrupt extension, signal 2
-	Interrupt extension, signal 3
-	Interrupt extension, signal 11
-	Interrupt extension, signal 12

3.3   AUTONOMOUS TRANSFER UNIT

3.3.1   General

The Autonomous Transfer Unit (ATU) permits an option of one to six peripherals to transfer words directly to and from the store by stealing store cycles. Connections between the peripherals and the ATU use the 900 Series Autonomous Interface; this is similar to the direct interface referred to in Section 2.14 but does not have the full addressing capability provided in the latter.   The ATU connects directly to the store data bus (described in Appendix D) and uses the central processor autonomous access facility described in Appendix C.

The ATU is connected to the computer-store highway as an autonomous access channel and also requires connection to the direct interface of the computer.   Up to four ATU's can, if required, be connected to one computer, thus permitting the connection of a total of 24 peripherals.

3.3.2   Mode of Operation

A sequence of transfers to and from a peripheral is initiated by an instruction obeyed by the processor.   The sequence can consist of any or all of the following:-

(a)   0 to 3 control word transfers to peripheral

(b)   0 to 4095 data word transfers to or from peripheral

(c)   A status word transfer from peripheral

The sequence proceeds autonomously until all transfers have been completed.   The peripheral may then interrupt the processor if it is ready for a new sequence.   A sequence of transfers can also be interrupted and terminated by a processor instruction to the ATU.

Sequences of transfers to the autonomously connected peripherals can be interleaved to allow concurrent operation.   At the end of each store cycle the peripheral channel signals are examined and the peripherals are serviced in a pre-determined priority.

Each peripheral attached to the ATU has associated with it four locations in the store; the contents of these are used in the sequence of transfers as detailed in 3.3.3

Location	Bits	Function
P	1 - 17	Data Pointer
	18	Output Indicator
P + 1	1 - 12	Data Count
	15	Cyclic Indicator
	13 - 14	Control Count
	16	Status Word Indicator
	17 - 18	(Spare)
P + 2	1 - 17	Control Pointer
P + 3	1 - 18	Status Word

The ATU contains count and address registers for each channel, and these are automatically loaded from the appropriate store location, when a sequence is initiated. The current contents of these count and address registers may be examined by the central processor.

3.3.3   Operational Sequence

Control Word Transfers take place from consecutive store locations whose starting address is given by the contents of location P + 2. The number of control word transfers in a sequence is controlled by bits 13 and 14 of location P + 1; these bits represent a count of the number of control words to be transferred as follows:-

Bits 14	Bits 13	No. of transfers
1	1	3
1	0	2
0	1	1
0	0	0

Data Transfers take place to or from consecutive locations whose starting address is given by the contents of location P. Bit 18 of location P is a 'one' to indicate output and a zero to indicate input. The number of data words transferred is controlled by bits 1 - 12 of location P + 1 which is loaded into the count register. If the number represented by these bits is X (where $X \neq 0$) the number of words to be transferred is X. The count register is decremented each time a data word is transferred. When X = 0 no further data transfers take place. During the last word of a data transfer a 'Last Word' signal is sent to the peripheral to indicate the end of a sequence.

<u>Cyclic Operation</u> occurs at the end of data transfer if bit 15 of the count register is a 1.   The address and count registers are automatically re-loaded from locations P + 1 and P, and the data transfer part of the sequence thus repeated. The loop is broken when the peripheral raises CONTROL READY in place of DATA READY thus causing a termination.   (See section 3.3.5).

A <u>Status Word Input</u> takes place if bit 16 of location P + 1 is a one; this bit is then cleared.   The status word is placed in location P + 3.

The store locations for each peripheral are as follows:-

	Channel No.					
	1	2	3	4	5	6
Data pointer	32	36	40	44	48	52
Indicators	33	37	41	45	49	53
Control pointer	34	38	42	46	50	54
Status word	35	39	43	47	51	55

For the second, third and fourth ATU's 32, 64, 96 respectively are added to the above addresses.

3.3.4   Program Control

A set of instructions are available to initiate or terminate a sequence on a particular channel.   In addition, the current state of a sequence may be examined by the processor.

Each peripheral may cause an interrupt if it is ready for a new sequence. Similar facilities to those described for the M.I.U. (Section 3.2) are available for inhibiting or enabling interrupts and identifying the source of interrupt.   An interrupt is cancelled by an Initiate Sequence instruction, and all interrupts are inhibited when the computer is reset.

15	5279 + N	Initiate sequence on channel N (N = 1 to 6)
15	5311 + N	Terminate sequence on channel N (N = 1 to 6)
15	5248	Allow interrupts on interrupt extension inputs as indicated by ones in Accumulator bits 1 - 12.

15	5249	Prohibit interrupts on interrupt extension inputs as indicated by ones in Accumulator bits 1 - 12.
15	1152	Place status of interrupt extension inputs into bits 1 - 12 of Accumulator
15	1153	Place into Accumulator bits 1 - 4 identification number of interrupt extension input causing interrupt. If more than one source of interrupt is simultaneously present the source connected via the patching connector to the lowest interrupt extension is indicated, the Accumulator is cleared if no interrupts are present.
15	1183 + N	Place Address Register of channel N (N = 1 to 6) into the accumulator, including output indicator.
15	1215 + N	Place Count Register of channel N (N = 1 to 6) into the accumulator, including status and cyclic indicators.

Instructions referring to the second, third and fourth ATU's have 8, 16 and 24 respectively added to all the above addresses.

3.3.5. Interfaces and Connections

Fig.14 shows the connection of an ATU into a 905 system. In addition to the outlets for each autonomous peripheral, the 905 direct peripheral interface is regenerated (SKT A) and a reduced set is regenerated on SKT B containing:-

Output Select	Reply
Address lines 1 and 7 - 11	Ready Y
Data Out 1 and 2	Reset
Power On	Mains failure

The ATU to peripheral interface (SKT C to H) contains the following signals:-

Data in   1 - 18

Data out 1 - 18

Address   1

Input Select

Output Select

Reply

Last Word

Data Ready

Control Ready (use optional)

Reset

Power On

Mask

The 'ready' lines are used by each peripheral to initiate a transfer. 'Data ready' initiates either a transfer of a data word or of a control word. 'Control ready' can only initiate a status input or control output transfer. If 'Control ready' is made true during a data input or output sequence when a 'Data ready' is expected, it causes premature termination of the sequence. When it occurs the next transfer is a Status Word Input (if the Status Word Indicator is true). The one bit cyclic indicator register is also cleared.

The mask line is intended to inform the peripheral that it is connected to an Autonomous Interface and not the Direct Interface. Address bit 1 denotes Data Input or Output if false and Control Output or Status Input if true.

The interrupt 'patching' socket L enables interrupt sources to be grouped and sent directly or through an interrupt 'mask' to the three central processor interrupts. In addition there are links to designate the ATU as the second, third or fourth unit.

3.3.6   Performance

For a 1 usec store the minimum transfer time for a word is 1.2 usecs plus the peripheral response time to select signals. This time can increase to 2.2. usecs should the ATU have to wait for a whole store cycle before gaining access to the store highway. The maximum rate of autonomous word transfer totalled over all ATU channels will be approximately 600 K words per second. The maximum word transfer rate for a single peripheral will be some 300 K words per second.

For a 2 usec store these transfer rates will be approximately 380 K words/second and 190 K words per second respectively.

3.3.7   Test Facilities

The ATU contains indicators and switches to aid fault finding. The facilities provided include:-

(1)   Inhibit switch for each peripheral channel

(2)   A means of inhibiting transmission and reception of store data highway signals by the ATU with simulation of 'accept' and 'store busy' signals.

(3)   Single cycle operation of the ATU

(4)   Monitor lamps for ATU registers

(5)   A means of simulating peripheral 'ready' and
        reply signals

(6)   Parity and Lock-out error display lamps and
        facilities for stopping the ATU when an error occurs

Off-line program testing can be carried out using a special cableform to connect the direct peripheral outlet to an ATU peripheral channel socket.

Program instructions allow the simulation and monitoring of transfers. The following instructions are used for off-line testing.

905 Instruction	Effect
15 1154	Monitor peripheral signals as follows:- Bits 1 - 6 Output Select on channels 1 - 6. Bits 9 - 14 Input Select on channels 1 - 6. (These signals are not monitored via the interface).
15 1155	Monitor peripheral signals on channel as follows:- Bit 1 Address Bit 1 Bit 2 Last Word Bit 3 Input Select Bit 4 Output Select (Bits 5 ÷ 18 Undefined)
15 5250	Generate ready signals on channel as follows:- Bit 1 Make Data Ready True Bit 2 Make Data Ready False Bit 3 Make Control Ready True Bit 4 Make Control Ready False
15 1156	Monitor data output signals on channel.
15 5251	Set input signals on channel according to Accumulator contents.

'Reply' is made true when either a 15   1156 or 15   5251 instruction is obeyed and false when 'select' is made false.   The second, third and fourth ATU's have 8, 16 and 24 respectively added to the above addresses.
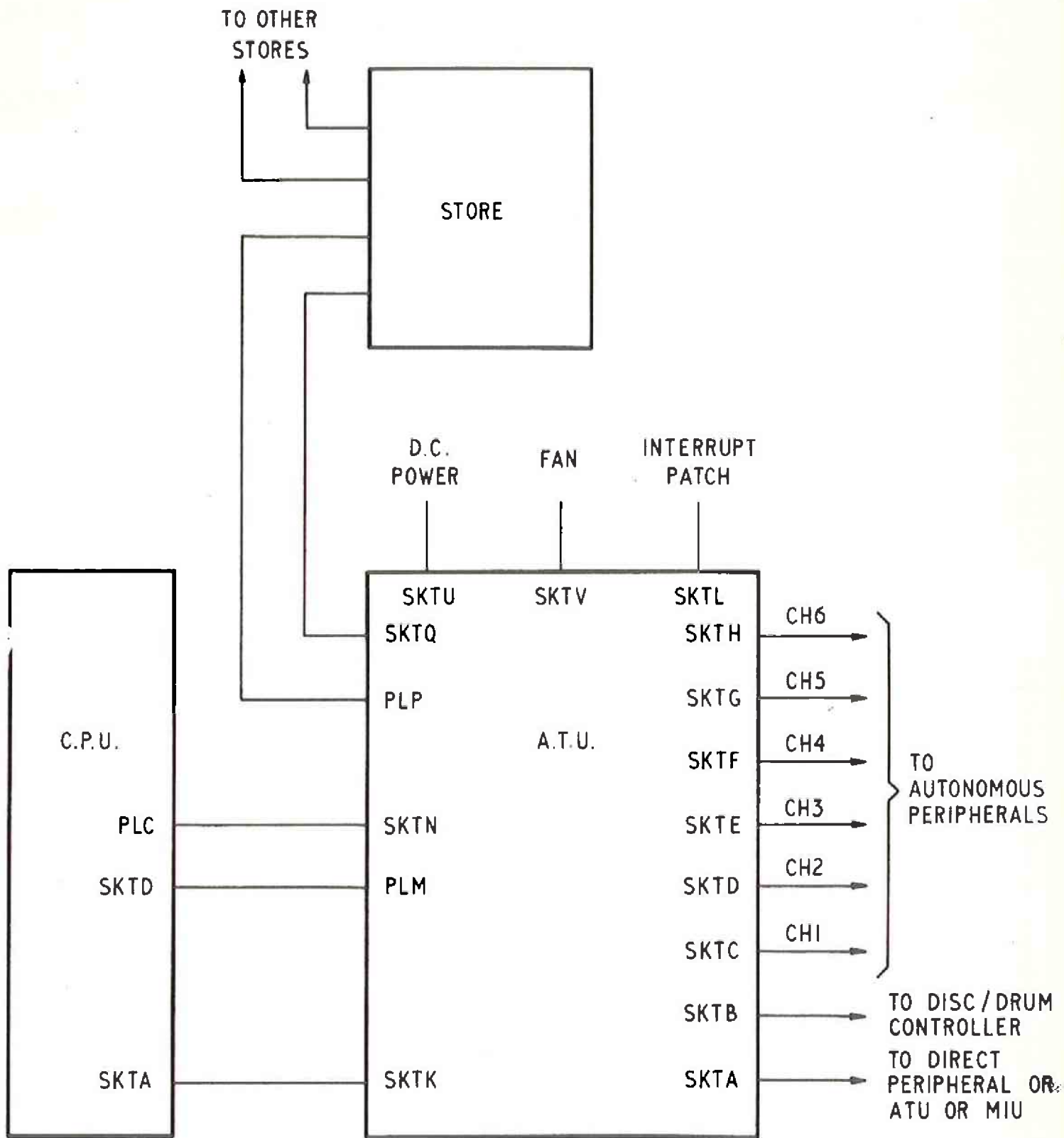
FIG. II   BLOCK DIAGRAM-905 SYSTEM WITH A.T.U.

3.3.8. Options

The ATU can be supplied in 2, 4, 6 or 8 channel versions. ATU options are also available with the logic associated with program interrupt omitted.

3.4 DUAL PROGRAM UNIT

3.4.1 Introduction

The Dual Program Unit is intended to allow the computer to be time-shared between one program which is fully checked out, and a second program which is under development, without affecting the integrity of the first program. The unit allows a "normal" mode of operation, and the operation of the dual program unit makes it impossible for this program to corrupt or hold up the first program. The normal program mode will in practice include an executive routine and one or more fully tested programs, which may be used for on-line control or off-line computing.

The slave mode will normally be used for development of one program, which may be in any stage of development, from initial testing to long-term trials. The development program cannot overwrite the store used by "normal" mode programs, or complete any input-output operations. Any attempt to do so will cause transfer to the executive routines which must take the appropriate action.

The development program may work off-line or on-line, providing that the executive program contains input/output routines for the appropriate peripherals. The developing program will normally arrange input/output by means of standard sub-routines or procedures, which hand over information to and from the executive.

3.4.2 Functional Specification

3.4.2.1 A one-bit memory within the unit controls the mode of operation.

When this memory is set to
normal mode all operations of the processor are as specified elsewhere
with the exception of the block transfer instructions which are not avail-
able when the dual program unit is attached.

When the unit is set to slave
mode, this causes a constant quantity (L) to be added to the addresses of
all store locations used by the processor (but not by autonomous access
channels).

The constant is a multiple of
4096 words and the effect of adding it to all store addresses is to render
locations with addresses less than L completely inaccessible to program.
Location 0 as used by a program operating in slave mode is thus in fact
location L.

The unit reverts to normal
mode when any of the following occur:

(a)   A location outside the available store is
         addressed.

(b)   Any input or output instruction is obeyed; in
         this case the instruction is not transmitted
         to any peripherals but is "trapped" by the
         DPU.

(c)   An interrupt signal is received.

In the cases of (a) and (b)
above an interrupt (normally on level 3) is generated by the DPU; details
of the occurrences are retained in an 18-bit status register included in
the DPU as follows:-

(a)   Location outside the available store:-

         Bits 1-17:   Address of location
         Bit 18:   "One"

(b)   Input or output instruction

         Bits 1-4:   Bits 1 to 4 of instruction address
         Bits 5-11:   Bits 5-11 of instruction address, if
                        general input-output instruction,
                        Zero if paper tape instruction.
         Bit 14:   "One" if general input instruction.
         Bit 15:   "One" if paper tape input instruction.

Bit 16:	"One" if general output instruction.
Bit 17:	"One" if paper tape output instruction.
Bit 18:	"Zero".

The interrupt generated in these circumstances will normally take place immediately following the instruction which caused it (unless it is a function 0 instruction following which interrupt cannot occur). The effects of references outside the available store are as follows:-

(a) Extraction of instruction - the instruction 14 0 will be obeyed (shift no places = do nothing).

(b) Extraction of operand - the pseudo-instruction 14 0 will be used as an operand.

(c) Storage of result - no effect on any store location, effects on registers as normal.

3.4.2.2   Instruction code

The following input-output instructions will be used to control the DPU.

15 6020   Prepare slave mode. Causes the DPU to switch to slave mode operation when program level 4 next becomes active, also clears the DPU status register.

15 6021   Resume normal mode. Causes a program interrupt on level 3 and hence normal mode operation to be resumed.

15 1924   Read DPU status. Causes the contents of the DPU status register to be copied into the accumulator. The contents of the register are not altered.

3.4.2.3   Program levels

It is implied above that slave mode operation can only occur when program level 4 (base level) is active. When any of levels 1, 2 or 3 become active as a result of interrupts normal mode operation is automatically resumed. When level 4 is active, slave mode operation will occur only if a 15 6020 instruction

was obeyed before a higher level was terminated, otherwise normal mode operation continues.

When slave mode operation is initiated by level 4 becoming active the S register is then loaded from location L+7 and the B register is held in location L+6.

3.5 DATA ROUTING UNITS

3.5.1 Data Routing Units

In a 905 system as previously described, a single 'data bus' links the processor, autonomous access channels and store units. Data routing units provide a means of generating additional data buses within a system and of providing links between these data buses. The units also provide a means of preventing a failure on one data bus from causing the complete failure of a system.

3.5.2 Data Routing Unit

A Data Routing Unit is connected to two data buses and provides a means of access from one to the other.

The two buses to which a DRU is connected are referred to as its "master" and "slave" buses respectively. It is connected to the master bus as a store unit and to the slave bus as an autonomous access channel. When a store cycle with an address within the range covered by the DRU is initiated on the master bus, the DRU requests access to the store on the slave bus. When this request is accepted, the DRU establishes a two-way connection between the master and slave buses and initiates a store cycle of the required type on the slave bus, thus a store unit attached to the slave bus can be accessed by the processor or other unit attached to the master bus.

The address range to which a DRU responds is normally 8192 words, the addresses which it accepts being identical to those which a store unit connected in its place on the master bus would accept. The slave store unit addressed will normally be the first unit on the slave data bus. Facilities are provided for varying the address range accepted, and the slave unit address generated by a DRU, by means of patch connections. The address range cannot exceed 32,768 words.

In the case of access to the slave bus not being possible, the DRU itself performs a pseudo store cycle and gives a failure indication to the master bus by means of simultaneous 'parity

error' and 'lock-out error' signals.   Under these circumstances the
pseudo-instruction 8 0 is generated as the 'contents' of the location
accessed.

3.5.3   Data Routing Control Unit

A Data Routing Control Unit again provides
a means of access from one data bus to another but also provides a means
of control of autonomous access to the second data bus.   It thus provides
a means of generating an independent data bus which is not directly con-
nected to a processor.

The two buses to which a DRCU is con-
nected are again referred to as its "master" and "slave" buses.   A store
cycle on the slave bus can be initiated by any one of four autonomous
access channels attached to the slave bus or by the initiation of a store
cycle on the master bus with an address in the range accepted by the
DRCU.   The DRCU accommodates four 'request' signals from the slave
autonomous access channels and generates 'accept' signals in return (in
the same way as the autonomous access control of the processor does).
In the event of simultaneous attempts to use the slave store the DRCU
assigns these on a fixed priority basis, thus:-

Autonomous Channel 1 - has highest priority and is accepted first.

Autonomous Channel 2 - is accepted only in the absence of a request
                       from channel 1.

Autonomous Channel 3 - is accepted only in the absence of a request
                       from channels 1 and 2

Autonomous Channel 4 - is accepted only in the absence of requests
                       from channels 1, 2 and 3.

In the absence of autonomous channel
requests, the DRCU can establish connection between the master and
slave and initiate a slave store cycle called for by the master bus.

The addressing arrangements and failure
detection features are identical to those of a DRU (see 3.5.2 above).   The
bus control and failure detection sections of a DRCU are kept entirely
separate so that a failure of one section does not involve failure of the
other.

3.5.4   System Configurations

Some typical configurations using the units
are shown in Figs. 12, 13 and 14.

The use of a Data Routing Control Unit
to provide an independent store for autonomous input/output is shown in
Fig. 13. The DRCU is used here to allow the processor and peripheral
store units to operate simultaneously except when cross reference between
them occurs, thus the input/output activity does not reduce the processor
throughput. This configuration is specially valuable for peripherals
which require repeated access to the same data (e.g. unbuffered displays,
line-printers).

Figs. 12 and 14 show dual processor
systems. In the first processor A has access to B's store but not vice-
versa; this is sufficient when the requirement is for messages to be
passed from one to the other. Where both processors require repeated
access to common storage the configuration shown in Fig. 14 is prefer-
able since references to the common store area by one processor stand
less chance of holding up the other.

(It is recommended that very complex
configurations of these units should be discussed with Elliott engineers
at the earliest opportunity.)

3.5.5   Performance

As with any autonomous store access
arrangement, the time required for an operation includes a variable
quantity to allow for the fact that the store may be at any point of its
operating cycle at the instant when a request is made; allowance must
also be made for higher priority accesses.

The effective times for store cycles
initiated on a master bus and performed on a slave bus are as follows:

Unit	Operation	Time			
		1 μs store		2 μs store	
		Min.	Max.	Min.	Max.
DRU	Read-restore	1.8 μs	2.8 μs	3.8 μs	5.8 μs
	Clear-write	2.0 μs	3.0 μs	4.0 μs	6.0 μs
DRCU	Read-restore	1.7 μs	2.7 μs	3.7 μs	5.7 μs
	Clear-write	1.9 μs	2.9 μs	3.9 μs	5.9 μs

The times for an autonomous store access
cycle performed on a bus controlled by a DRCU are the same as those
for a bus controlled by a processor (see Appendix C).

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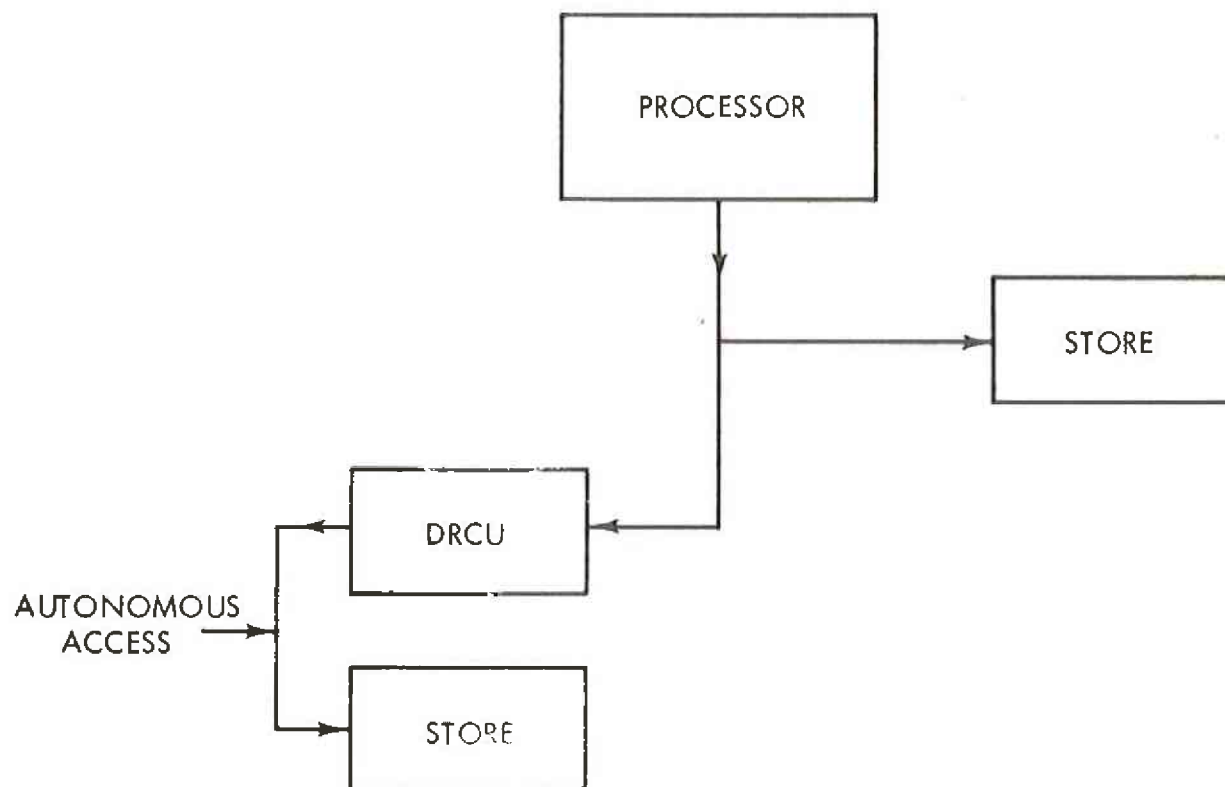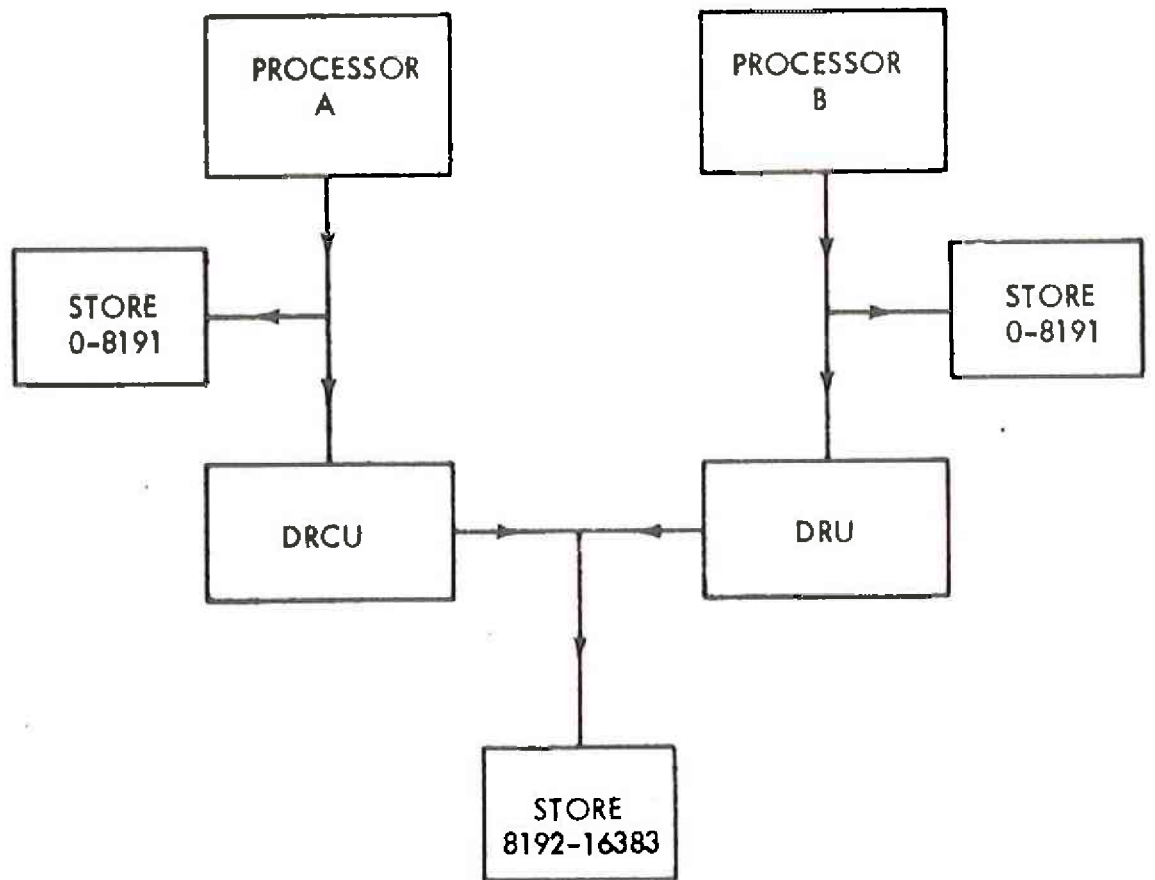905 INTER-COMPUTER CONNECTIONS   Fig. 12
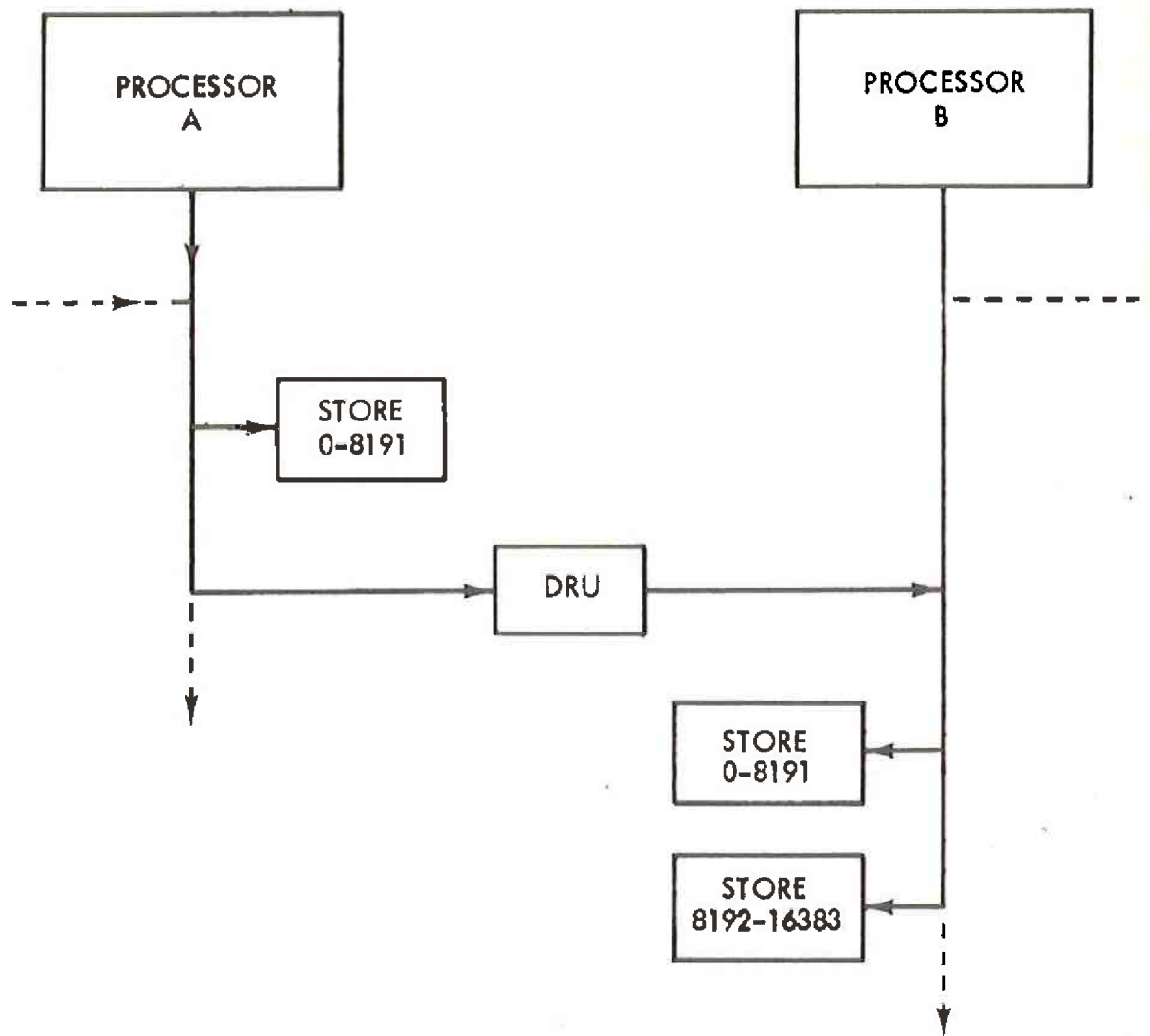
Fig. 13

Fig. 14

3.6   10 bit Analogue Input/Output Interface

3.6.1   General

This unit converts up to 8 or 16 analogue voltages into 10-bit digital data for input via the 905 direct I/O interface, and provides up to 8 analogue output channels from that interface.

3.6.2   A.D.C. Characteristics

Input voltage:	$\pm$ 10 volts full scale
Input Impedance:	100 M ohms
Source Impedance:	2 K ohms max
Aperture Time:	100 nanoseconds (max)
Accuracy:	Within 0.1% full scale
Linearity:	0.1% $\pm$ $\frac{1}{2}$ L.S.B.
Long term drift	0.1% per 30 days
Temperature Range:	0° C to 40° C
Temperature Coefficient:	25 ppm $/^{o}$ C
Digital Notation.	Two's complement, fractional

$+\frac{1}{2}$ full scale	0	100000000
Zero	0	000000000
$-\frac{1}{2}$ full scale	1	100000000

Throughput:	Up to 50 KHz

3.6.3   A.D.C. Operation

The analogue input signals can be sampled by computer program in a sequential or random sequence. Where the number of ADC channels in use is less then the 16 available the sequential mode can be "short sequenced", by altering wire links within the unit. Channel zero then follows the highest channel number in use.

The A.D.C. sample and conversion time is 20 microseconds. In the sequential mode, the conversion for the next channel proceeds immediately on input of the value for the current channel. In the random mode the current channel is re-sampled immediately on input of the current value to the computer. A value for a newly selected channel in the random mode is available 20 μsecs after the "set channel number" (control output) instruction (see 3.6.4).

The action of the interface RESET signal is to preset the A.D.C. to the random mode, with channel zero selected. The value given by the A.D.C. converter will be undefined.

3.6.4   A.D.C. Instructions

The instructions and word formats are as follows:-

1. Control Output 15 4737

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
X	X	X	X	X	X		X	X	X	X	X	X	X	N	N	N	N

a) Set mode; Random '0'
   Sequential '1'

b) Channel Number

2. Data Input 15 640 D$_s$ D$_s$ D$_s$ D$_s$ D$_s$ D$_s$ D$_s$ D D D D D D D D D 0 0

Regenerated Sign bit
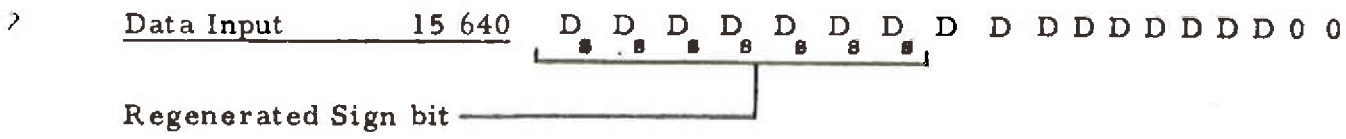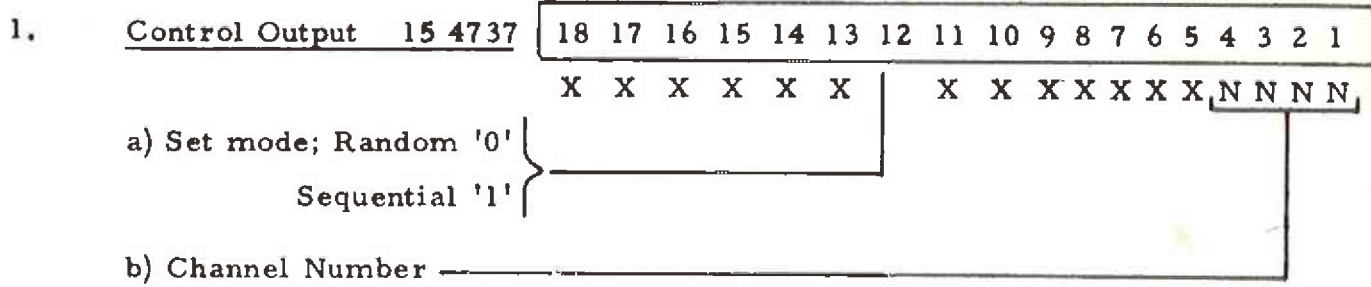
If in sequential mode, channel number incremented.

3. Status Input 15 641 0 0 0 0 0 0 | 0 0 0 0 0 0 0 N N N

a) Read Mode; Random '0'
   Sequential '1'

b) Channel Number

3.6.5   D.A.C. Characteristics

Output voltage:	$\pm$ 10 volts full scale
Output Current:	5 ma at 10 volts
Output Impedance:	0.1 ohm at D.C.
Settling time:	25μ secs for 10 volts to 0.1%
Accuracy:	0.1%
Temperature Range:	0°C to 40°C
Temperature Coefficient:	25 ppm / °C
Digital notation:	two's complement, fractional
+ ½ full scale	0 100000000
zero	0 000000000
- % full scale	1 100000000

3.6.6   D.A.C. Operation

The D.A.C. channels may be updated in a sequential or random manner. When the number of DAC channels in use is less than the maximum available, the sequential mode can be "short sequenced", channel zero following the highest channel number used, by altering wire links in the unit.

3.6.6 Cont'd.

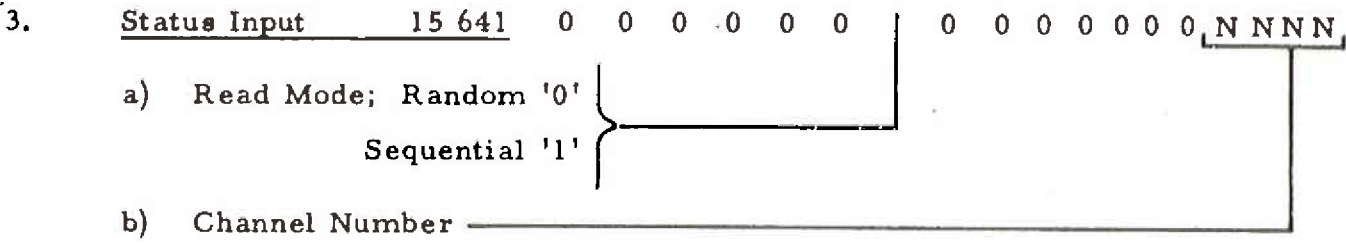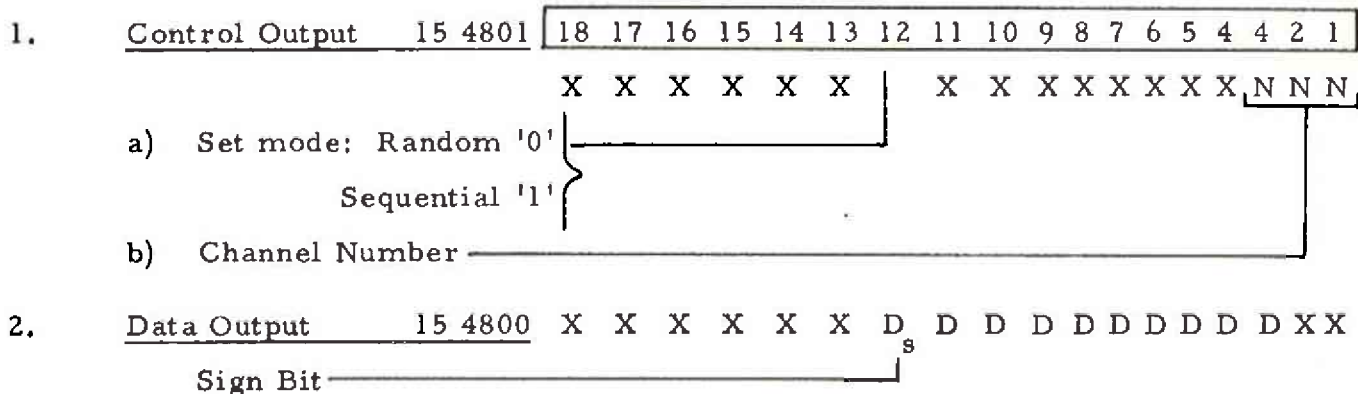A D.A.C. program instruction may be obeyed at any time. The response time to instructions is not dependent upon the conversion and settling time.
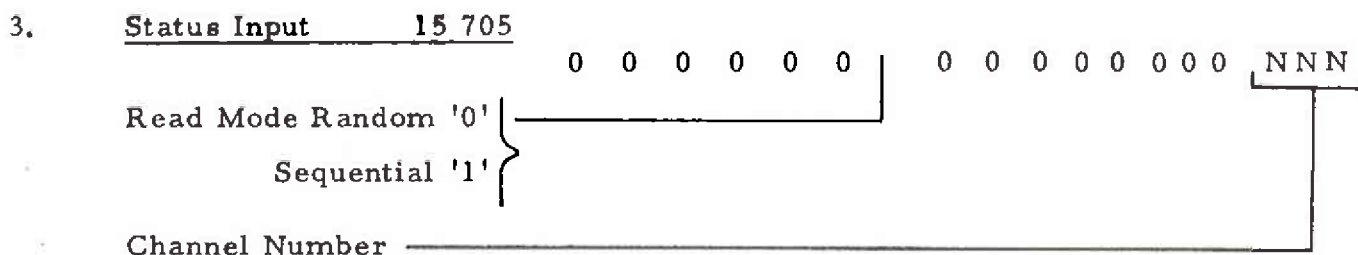
The action of the interface RESET signal is to preset the D.A.C. to the random mode, with channel zero selected. Each D.A.C. channel value will be set to zero.

3.6.7 D.A.C. Instructions

The instructions and word formats are as follows:-

1. Control Output   15 4801

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	4	2	1
X	X	X	X	X	X		X	X	X	X	X	X	X	N	N	N

a) Set mode: Random '0'
                      Sequential '1'

b) Channel Number

2. Data Output   15 4800   X X X X X X D_s D D D D D D D D X X

    Sign Bit

If in sequential mode, channel number is incremented.

3. Status Input   15 705

    0 0 0 0 0 0   0 0 0 0 0 0 0 0 N N N

Read Mode Random '0'
             Sequential '1'

Channel Number

3.7   REAL TIME CLOCKS

Two types of interrupt generators are available. The first, for use in conjunction with the ADC and DAC unit described above, allows the interrupt rate to be preset by wire links over the range of 1 to 16, 384 times per second.

The second type, normally used in conjunction with the Multiplex Interrupt Unit, can have its interrupt rate varied by program action, and elapsed time may be read from a counter within the unit.

3.8   INSTALLATION

An extended 905 system consists basically of a desk unit 42 in wide x 36 in high x 26 in deep (Fig. 9) to which may be added extension cabinets of the type shown in Fig. 8.

Appendix A: INITIAL INSTRUCTIONS

        Locations 8180 to 8191 inclusive are used to contain the
initial instructions. These instructions are brought into use when a
program is entered and remain in use until a 15 7168 or 15 7177
instruction is obeyed. While the instructions are in use the contents of
the locations are fixed and cannot be changed in any way. The locations
can be used normally after one of the above instructions has been
obeyed. The sequence of the instructions is as follows:

8180	/15	8189	8186	15	2048
8181	0	8180	8187	/ 5	8180
8182	4	8189	8188	10	1
8183	15	2048	8189	4	1
8184	9	8186	8190	9	8182
8185	8	8183	8191	8	8177

ISO Code Value	Value with Parity	Telecode Character (General)	Binary Pattern	Teleprinter		Notes for Other Devices
				Keys Pressed to Transmit	Effect when Received	
0	0	blank	00000.000	Run out	no effect	
1	129		10000.001	A & control	no effect	
2	130		10000.010	B & control	no effect	
3	3		00000.011	C & control	no effect	
4	132		10000.100	D & control	no effect	
5	5		00000.101	E & control	no effect	
6	6		00000.110	F & control	no effect	
7	135	Bell	10000.111	G & control	Bell	(Ignored by **Flexo**-writer
8	136		10001.000	H & control	no effect	
9	9	Hor. Tab.	00001.001	Tab.(I & control)	no effect	
10	10	Line feed	00001.010	Line feed	Line feed	New line on Flexo-writer
11	139		10001.011	& control	no effect	
12	12		00001.100	& control	no effect	
13	141	Car. Retn	10001.101	Return	Car. Retn	(Ignored by Flexo-writer
14	142		10001.110	N & control	no effect	
15	15		00001.111	O & control	no effect	
16	144		10010.000	P & control	no effect	
17	17		00010.001	Q & control	no effect	
18	18		00010.010	R & control	no effect	
19	147		10010.011	S & control	no effect	
20	20	Halt	00010.100	Halt (T & control)	no effect	(Stops Flexo-writer
21	149		10010.101	U & control	no effect	
22	150		10010.110	V & control	no effect	
23	23		00010.111	W & control	no effect	
24	24		00011.000	X & control	no effect	
25	153		10011.001	Y & control	no effect	

ISO Code Value	Value with Parity	Telecode Character (General)	Binary Pattern	Teleprinter		Notes for Other Devices
				Keys Pressed to Transmit	Effect when Received	
26	154		10011.010	Z & control	no effect	
27	27		00011.011	K Shift & Control	no effect	
28	156		10011.100	L Shift & Control	no effect	
29	29		00011.101	M Shift & Control	no effect	
30	30		00011.110	N Shift & Control	no effect	
31	159		10011.111	O Shift & Control	no effect	
32	160	Space	10100.000	Space bar	Space	
33	33	!	00100.001	! (1 & shift)	!	Ignored by Flexo-writer
34	34	"	00100.010	" (2 & shift)	"	
35	163	$\frac{1}{2}$	10100.011	$\frac{1}{2}$ (3 & shift)	$\frac{1}{2}$	
36	36	$	00100.100	$ (4 & shift)	$	
37	165	%	10100.101	% (5 & shift)	%	
38	166	&	10100.110	& (6 & shift)	&	
39	39	´(acute)	00100.111	´ (7 & shift)	´	
40	40	(	00101.000	((8 & shift)	(	
41	169	)	10101.001	) (9 & shift)	)	
42	170	*	10101.010	* (: & shift)	*	
43	43	+	00101.011	+ (; & shift)	+	
44	172	,	10101.100	,	,	
45	45	-	00101.101	-	-	
46	46	.	00101.110	.	.	
47	175	/	10101.111	/	/	
48	48	0	00110.000	0	0	
49	177	1	10110.001	1	1	
50	178	2	10110.010	2	2	
51	51	3	00110.011	3	3	
52	180	4	10110.100	4	4	
53	53	5	00110.101	5	5	
54	54	6	00110.110	6	6	
55	183	7	10110.111	7	7	
56	184	8	10111.000	8	8	
57	57	9	00111.001	9	9	
58	58	:	00111.010	:	:	
59	187	;	10111.011	;	;	
60	60	<	00111.100	<	<	
61	189	=	10111.101	=	=	

ISO Code Value	Value with Parity	Telecode Character (General)	Binary Pattern	Teleprinter		Notes for Other Devices
				Keys Pressed to Transmit	Effect when Received	
62	190	>	10111.110	>	>	
63	63	1o (suffix)	00111.111	1o	1o	
64	192	`(grave)	11000.000	`(P & shift)	`	
65	65	A	01000.001	A	A	
66	66	B	01000.010	B	B	
67	195	C	11000.011	C	C	
68	68	D	01000.100	D	D	
69	197	E	11000.101	E	E	
70	198	F	11000.110	F	F	
71	71	G	01000 111	G	G	
72	72	H	01001.000	H	H	
73	201	I	1100 001	I	I	
74	202	J	11001.010	J	J	
75	75	K	01001.011	K	K	
76	204	L	11001.100	L	L	
77	77	M	01001 101	M	M	
78	78	N	01001 110	N	N	
79	207	O	1001.111	O	O	
80	80	P	01010 000	P	P	
81	209	Q	11010.001	Q	Q	
82	210	R	11010.010	R	R	
83	83	S	01010.011	S	S	
84	212	T	11010.100	T	T	
85	85	U	01010 101	U	U	
86	86	V	0 1 0	V	V	
87	215	W	110 0.111	W	W	
88	216	X	1011.000	X	X	
89	89	Y	01011.001	Y	Y	
90	90	Z	01011.010	Z	Z	
91	219	[	1 1.011	[(K & shift)	[	
92	92	£	010 .100	£ (L & shift)	£	
93	221	]	1 1.101	] (M & shift)	]	
94	222	↑	1 1.110	↑ (N & shift)	↑	
95	95	←	0 1.111	← (O & shift)	←	(Ignored by Flexo _writer

ISO Code Value	Value with Parity	Telecode Character (General)	Binary Pattern	Teleprinter		Notes for Other Devices
				Keys Pressed to Transmit	Effect when Received	
96	96	@	01100.000	-	\	
97	225	a	11100.001	-	A	
98	226	b	11100.010	-	B	
99	99	c	01100.011	-	C	
100	228	d	11100.100	-	D	
101	101	e	01100.101	-	E	
102	102	f	01100.110	-	F	
103	231	g	11100.111	-	G	
104	232	h	11101.000	-	H	
105	105	i	01101.001	-	I	
106	106	j	01101.010	-	J	
107	235	k	11101.011	-	K	
108	108	l	01101.100	-	L	
109	237	m	11101.101	-	M	
110	238	n	11101.110	-	N	
111	111	o	01101.111	-	O	
112	240	p	11110.000	-	P	
113	113	q	01110.001	-	Q	
114	114	r	01110.010	-	R	
115	243	s	11110.011	-	S	
116	116	t	01110.100	-	T	
117	245	u	11110.101	-	U	
118	246	v	11110.110	-	V	
119	119	w	01110.111	-	W	
120	120	x	01111.000	-	X	
121	249	y	11111.001	-	Y	
122	250	z	11111.010	-	Z	
123	123		01111.011	-	[	
124	252		11111.100	-	no effect	no effect on Flexo- writer
125	125		01111.101	-	no effect	
126	126		01111.110	-	no effect	
127	255	delete	11111.111	delete	no effect	

85
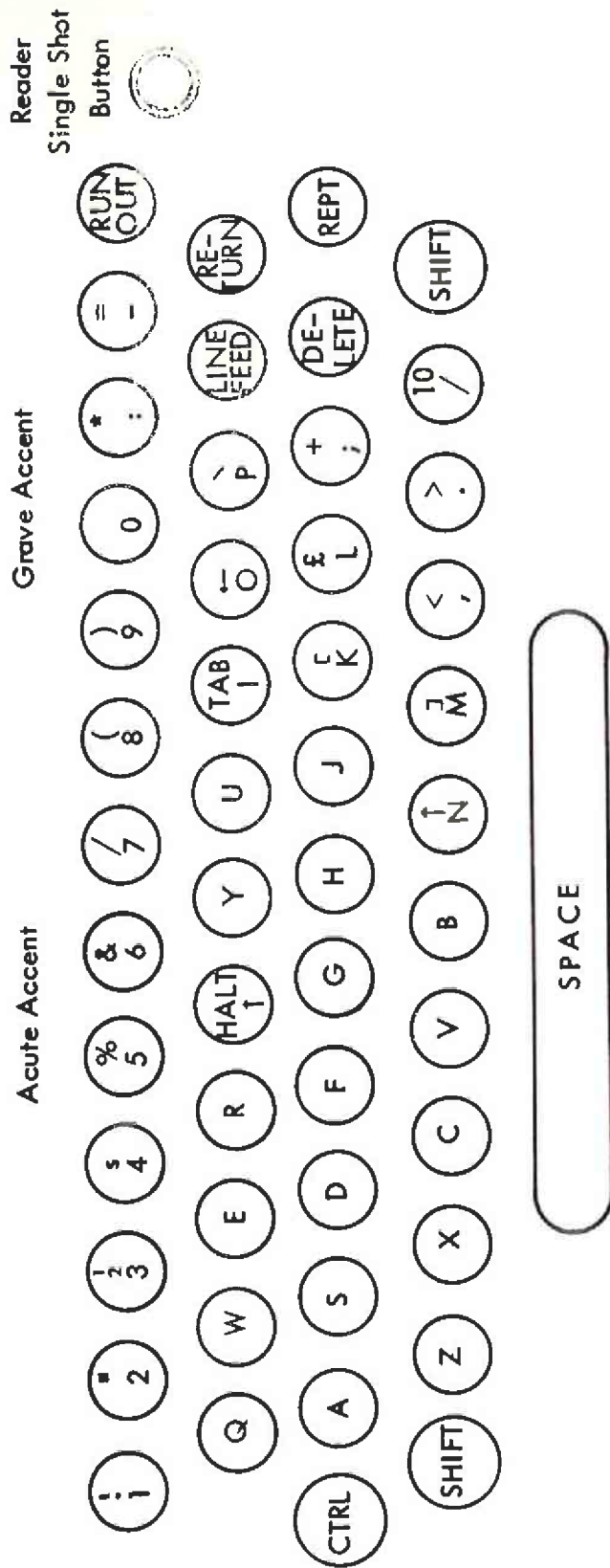
TELEPRINTER KEYBOARD LAYOUT   Fig. 15

Appendix C: AUTONOMOUS ACCESS FACILITY

1.   This allows information to be transferred between the store and peripheral devices without using the processor. Information is extracted from and placed in the store by 'stealing' store cycles, hence data transfers are interleaved with normal computing.

Units using this facility, referred to as autonomous access channels, are connected to the 'data bus' lines which interconnect the processor and store units. Lines carrying signals to the store are thus fed by the processor and autonomous access channels in parallel and feed the store units also inparallel. Similarly, lines carrying signals from the store are fed by the store units in parallel and feed autonomous access channels and the processor in parallel.

Control Logic located in the processor regulates the use of the 'data bus' system. An autonomous access channel requiring to perform a transfer sends a 'request' signal to the control logic. At the end of each store cycle the control logic examines the 'request' signals and sends an 'accept' signal to one autonomous access channel, allowing the channel to perform one complete store cycle.

2.   Four 'request' signals from four autonomous access channels are accommodated by the control logic; in the event of simultaneous requests from different channels the control logic accepts these on a fixed priority basis, i.e.

Channel 1 has highest priority and is accepted first

Channel 2 is accepted only in the absence of a request from channel 1

Channel 3 is accepted only in the absence of requests from channels 1 and 2

Channel 4 is accepted only in the absence of requests on other channels

If no requests are waiting the processor can access the store.

3.   Operation Times

The time for an autonomous access operation can be divided into two parts, the response time (from the sending of the 'request' signal until the 'accept' signal is received) and the store operation time. The response time includes the time for the store to complete an operation in progress when the request is received. Total operation times for the transfer of one word into or out of the store on channel 1 (highest priority) are:-

	1µs store	2µs store
Minimum	1.5µs	2.5µs
Maximum	2.7µs	4.7µs

For other channels, the response time will be increased when higher priority channels simultaneously make requests. When the maximum possible data transfer rate is required, it is possible for channel 1 to use a number of successive store cycles, hence the maximum rates are:-

with 1µs store 15.10^6 bit/s (833,333 words/s)
with 2µs store 8.18^6 bit/s (454,545 words/s)

Appendix D: STORE INTERFACE

The connectors feed out to a data bus system, which can also be used for data transfers directly to autonomous access channels. Each channel may feed a peripheral capable of corresponding with the store directly; or a less complex peripheral device, via an Autonomous Transfer Unit. In either case, data is transferred without passing through the processor and logic circuitry in the processor regulates the access to store on a priority basis.

The processor to store interface therefore contains some signal lines only relevant to the autonomous access channels.

Timing diagrams are shown in Figs. 16, 17 and 18.

1.   Data Transfer

Transfer of data between store and processor will be in a parallel binary mode and will have a word width of 18 bits. The maximum data transfer rate is 833,333 words per second.

Data entering the store is duplexed with the store location address, thereby reducing the number of lines involved.

2.   Data Transfer Timing

2.1   Data from Store

When an input is required by the processor, it will send a 'Select Store' signal along the store line, and also the address of the store location required. A 'Trigger Read' signal and a 'Permit Write' signal will then be transmitted to the store, and the processor will await a 'Read Busy' signal from the store.

The start of data transfer from the store will be indicated by the ending of the 'Read Busy' signal. During the data transfer a 'Write Busy' signal will be sent from the store, and the ending of this signal will occur before the cessation of the data being transferred at the end of the cycle.

2.2   Data to Store

When an output is required by the processor, it will send a 'Select Store' signal along the store bus, and also the address of the store location required. The processor will then transmit 'Trigger Read', 'Permit Write' and 'Inhibit Read Out' signals to the store, and will await a 'Read Busy' signal from the store.

When the processor receives 'Read Busy', the address information will be removed from the duplexed lines and the data to be transferred substituted. During the data transfer a 'Write Busy'

signal will be sent from the store and the ending of this signal will cause the cessation of the data being transferred.

3. Interface Signals

The functions and directions of the signals on the interconnecting lines at the interface are given below. The states of the lines carrying binary data are described as ONE or ZERO, and those lines carrying logic or controlling functions, as TRUE or FALSE.

3.1 Store Select

From computer, eight lines. A line when set true will allow the appropriate store unit to respond to control signals. It becomes false when the 'Address' lines are set to their zero state. Each line is normally false when the appropriate store is not being accessed.

3.2 Address and Data Output

From computer, eighteen lines. Fourteen of the lines are duplexed, carrying both the address and data information. Each duplexed line will be in its correct state for the address bits at the same time as 'Store Select', and will become zero after the start of 'Read Busy' and before the end of 'Trigger Read'.

The lines will remain zero for a short duration after transmitting the address. All eighteen lines will then be set to their correct state for the binary word to be transferred, and will remain correct until the end of 'Write Busy'.

3.3 Trigger Read and Permit Write

From computer, one line each. Both signals will only become and remain true when 'Store Select' is true, and when the 'Address' lines are in their correct state.

The lines are normally false when the store is not being accessed.

3.4 Inhibit Read Out

From computer, one line. This line will only become and remain true, when 'Trigger Read' is true and when data is required to be written into store.

The line is normally false when the store is not being accessed.

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3.5   Read Busy

To computer, one line.   This line will be set true when 'Trigger Read' is true, and will become false when the 'Data Output' lines are set to their correct state.

The line is normally false when the store is not being accessed.

3.6   Write Busy

To computer, one line.   This line will be set true when 'Read Busy' has become false, and during the time that the 'Data output' lines are set to their correct state.   It will become false before 'Data Input' or 'Data Output' are set to their zero state.

The line is normally false when the store is not being accessed.

3.7   Data Input

To computer, eighteen lines.   The lines will be set to their correct state when 'Read Busy' becomes false, and before 'Write Busy' is set true.   The data input information will remain established until the end of the cycle.

The lines are normally in the zero state and are only set otherwise when the store is being accessed.

3.8   Parity Error

To computer, one line.   The line will only be set true when the parity of the data information to be transferred is not correct.   In such an event the signal will be set about 150 nanoseconds after the establishment of the data by the store, and will remain true until the end of the cycle.

3.9   Lock Out Error

To computer, one line.   The line will only be set true if a protected location of the store is addressed, when attempting to write data into store.   In such an event, the signal will be set about 100 nanoseconds after the establishment of the address information, and will remain true until the end of the cycle.

3.10 Store Reset

From computer, one line.   The line will be set false when the computer is first switched on, and if in the 'Auto' mode, will become true when the various interlocks clear.   On switching on in the 'Manual' or 'Test' mode, the line will be set false continuously until

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the 'Jump' control is operated. The line will also be set false continuously when the 'Jump' control is operated. The line will also be set false continuously when the 'Reset' control is operated (in the 'Manual' or 'Test' mode) and will only become true on operation of the 'Jump' control.

The line will normally be set true but will become false when switching on the computer, or if a line voltage or store temperature fault condition occurs.

3.11 Lockout

From computer, one line. The line when set false will not allow protected store locations to be over-written.

The line will normally be set false, but may be set true in 'Manual' or 'Test' operating modes, whereupon data may be written into any store location.

3.12 Interlock

To computer, one line. The line will be set true when store voltage and temperature are within limits. The line will normally be true, and will only become false when a fault occurs.

3.13 Interlock In

From computer, one line. This line will be energised when power is applied to the central processor and will be de-energised when power is removed.

3.14 Autonomous Access Channel: Request

To computer, four lines. A line when set to the true state will indicate to the processor that there is an autonomous channel requiring access to store. Towards the end of each store cycle, all 'Request' signals will be examined on a priority basis to allow a store access to the data bus system.

The 'Request' signal remains true until the appropriate 'Accept' signal is received. The line is normally false.

3.15 Autonomous Access Channel: Accept

From computer, four lines. A line, when set true, will allow the appropriate autonomous channel unhindered access to store for one complete cycle.

The 'Accept' signal will remain true until the end of the cycle, and at all other times when not accessing store, will be false.
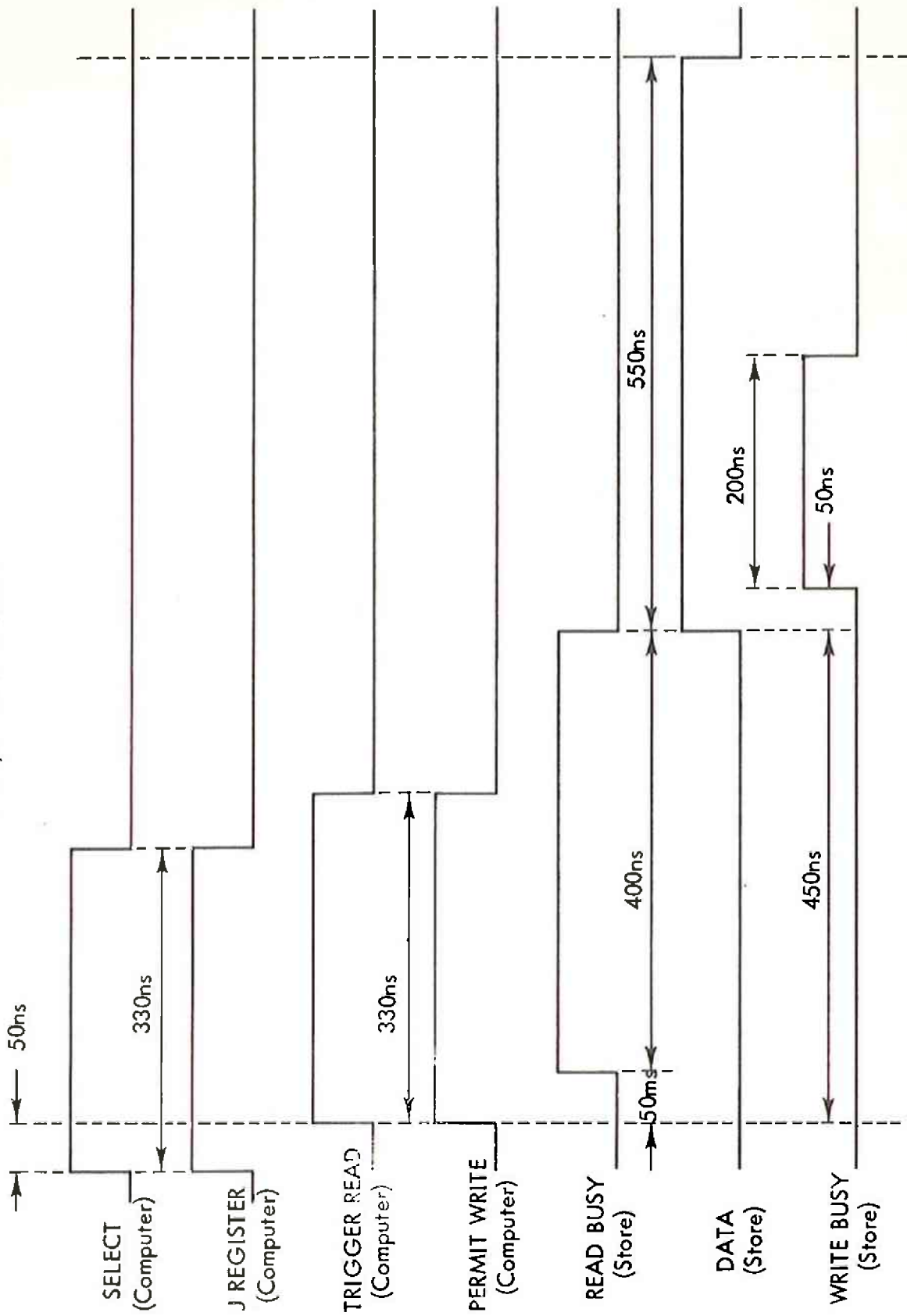
3.16 Program Level Information

From computer, two lines. The state of these lines, 'E2' and 'E3', will indicate the current level of program, and are provided for a multi-programming facility.

3.4.4 Store Transmitters and Receivers

The central processor contains transmitters and receivers that make direct connection with the signal lines interconnecting the store bus system with the computer. The circuits are shown on drawing MSA 4314, obtainable from Mobile Computing Division.

READ/RESTORE CYCLE

SELECT (Computer)
J REGISTER (Computer)
TRIGGER READ (Computer)
PERMIT WRITE (Computer)
READ BUSY (Store)
DATA (Store)
WRITE BUSY (Store)

50ns
330ns
330ns
400ns
550ns
200ns
50ns
450ns
50ns

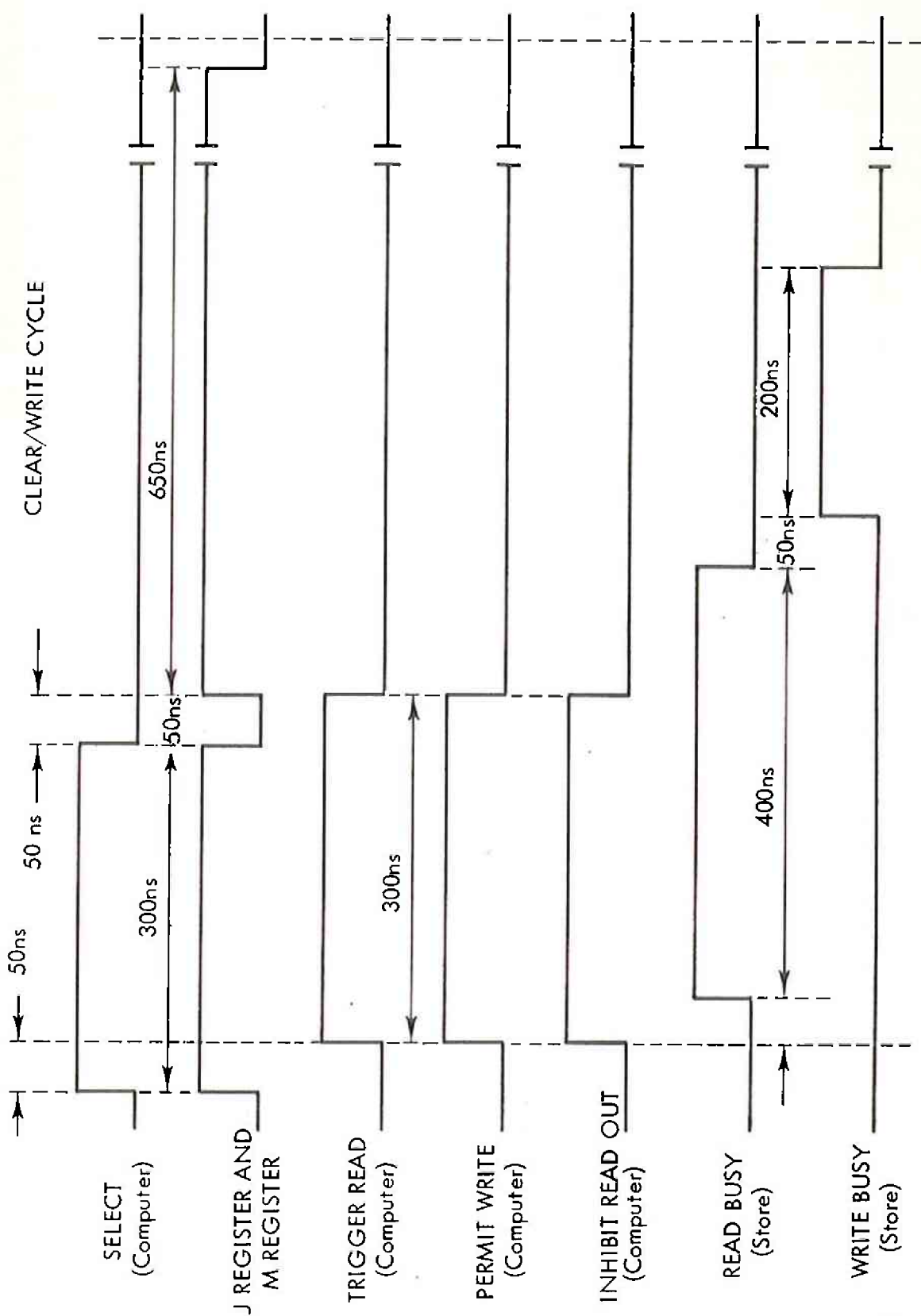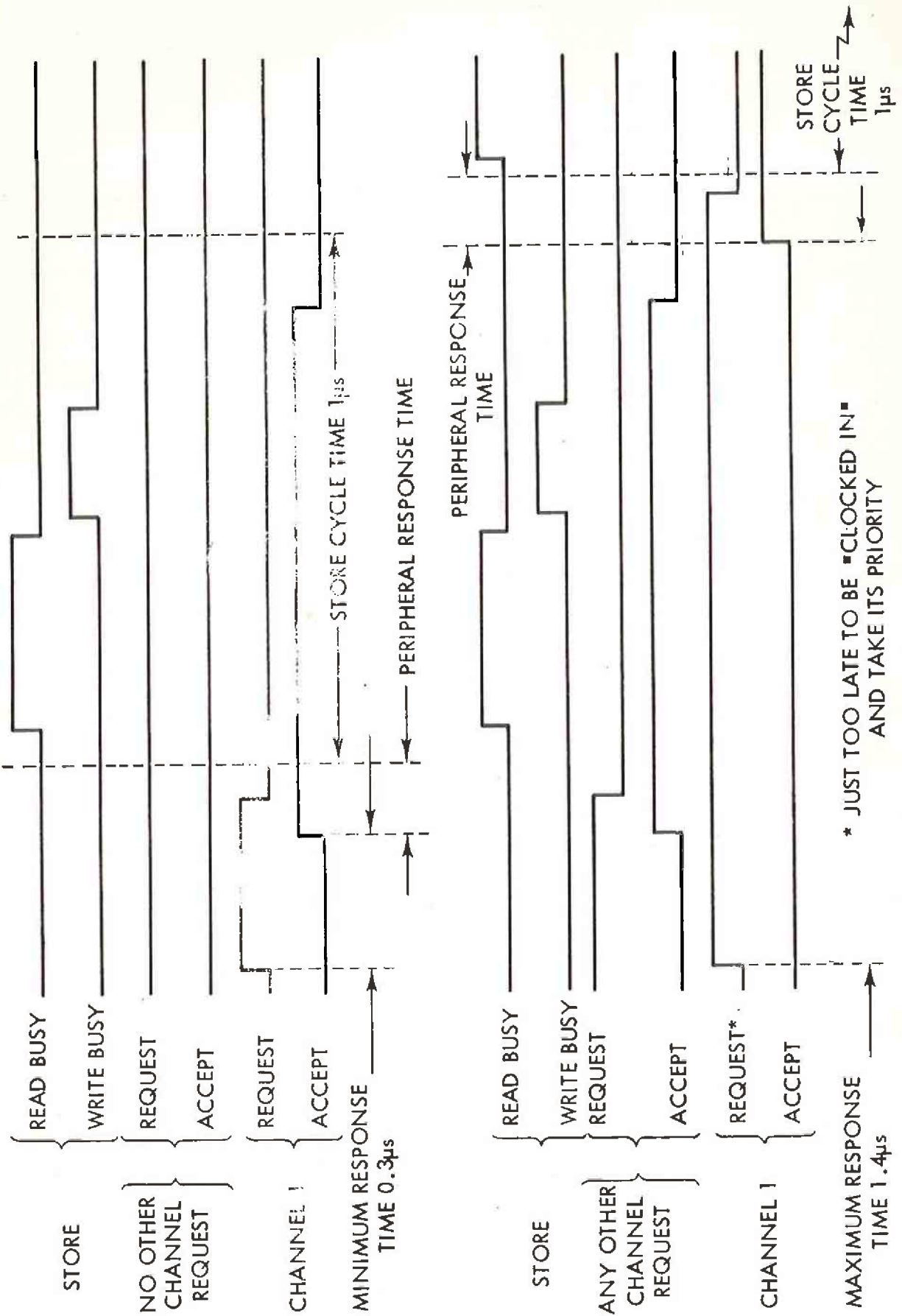DATA INPUT TIMING

Fig.16

Fig. 17   DATA OUTPUT TIMING

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AUTONOMOUS ACCESS RESPONSE TIMING   Fig.18

OPT/905/4.69/2

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